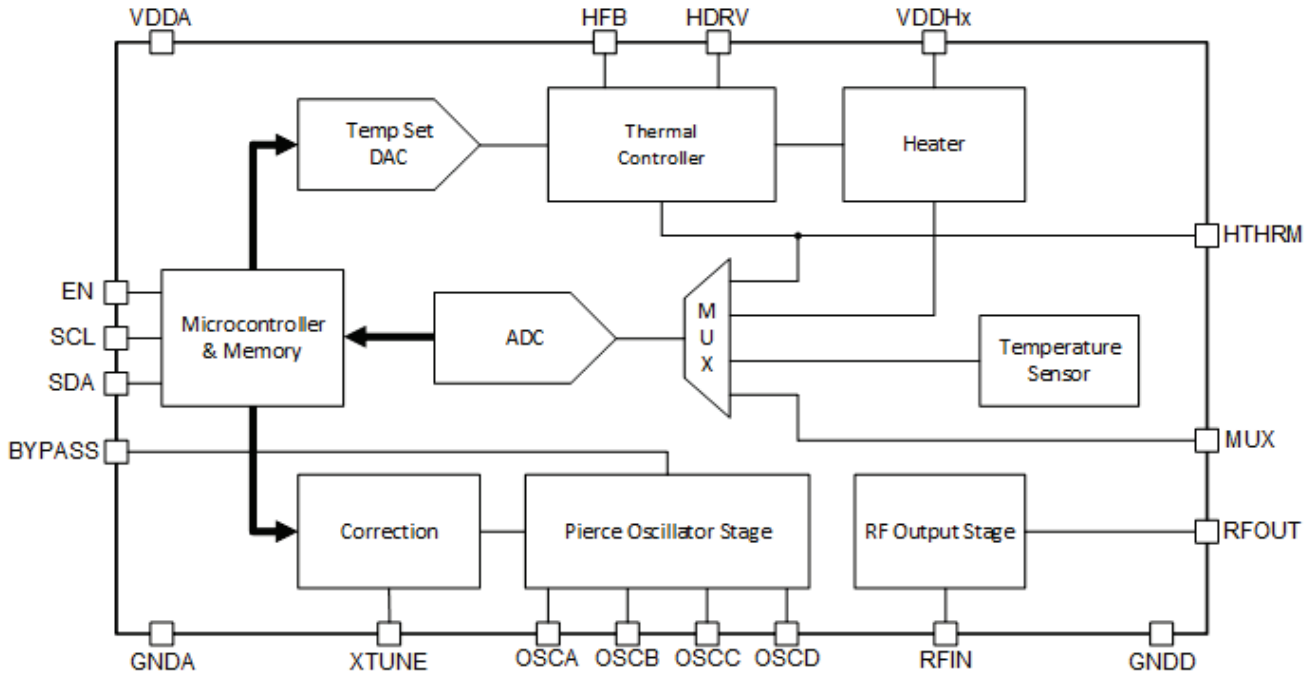
# OCXO Core IC

## Description

The TM200 is a fully integrated programmable thermal management unit that monitors, controls, and corrects analog circuitry across a wide temperature range. The TM200 is primarily intended for OCXO applications and includes a temperature sensor, internal Pierce oscillator & output stage, thermal controller, internal heater and data converters in conjunction with a microcontroller (MCU) and memory structures. The TM200 controls and regulates the temperature environment of small enclosures by executing temperature stability and correction programs. The integrated Pierce oscillator and output stage are designed to be flexible with a variety of oscillator and crystal configurations. The IC includes many programmable functionality options and has an accompanying software package that configures the IC for the desired thermal characteristics. It communicates via an I²C interface and is available in an 3mm x 3mm package or as die.

## Block Diagram




## Features

- Low phase noise oscillator
- Low Allan deviation for high stability clocks
- High accuracy temperature sensor
- Controls internal (1W) or external heaters

## Applications

- OCXO Modules
- Thermal Protection & Management
- Environmental Control Systems
- Precision Measurement

## Ordering Information

| Order Number | Package | Quantity | RoHS | MSL Rating | Leadframe |
|---|---|---|---|---|---|
| TM200-T1 | 20L STSLP QFN | 123 | Yes | 1 | NiPdAu |
| TM200-R1 | 20L STSLP QFN | 1000 | Yes | 1 | NiPdAu |
| TM200-X | Die | TBD | n/a | n/a | n/a |

# SPECIFICATIONS

## Environmental Specifications

**Table 1 Recommended Operating Conditions**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | VDDA ± 5% | 3.135 | 3.3 | 3.465 | V |
| Operating Temperature | | -40 | | 125 | °C |
| OTP Programming Temperature | | 0 | | 50 | °C |

## Temperature Sensor Specifications

**Table 2 Temperature Sensor Specifications**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Absolute Accuracy | | -0.25 | | 0.25 | °C |
| Voltage Range | -40C to 125C | 1.32 | | 2.5 | V |
| Resolution | ADC LSB | | 0.11 | | °C |
| Linearity | -40C to 125C | | 0.6 | | % |
| | 70C to 125C | | 0.2 | | |

## Thermal Controller Specifications

**Table 3 Thermal Controller Specifications**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Internal Heater Current | -40C | 160 | | 267 [1] | mA |
| | 100C | 160 | | 221 [1] | |
| | 125C | 160 | | 211 [1] | |
| Continuous Internal Heater Power | 3.3V Supply (VDDHx) | | | 0.5775 [2] | W |
| Thermal Controller Output Drive Range | Internal Heater | 0 | | VDDA - 0.1 | V |
| | External Heater | 0 | | VDDA - 0.1 | |
| Thermal Controller Drive Current | External Heater | 7 | 8.1 | | mA |
| Thermal Controller Feedback Range | Internal Heater | 0 | 0.653 | 0.782 | V |
| | External Heater | 0 | | 2.9 | |
| Current Limiter DAC Reference | | | 2.9 | | V |
| Current Limiter DAC Resolution | | | 7 | | bits |
| Current Limiter DAC Codes | | | 128 | | steps |
| Current Limiter DAC LSB | | | 22.7 | | mV |
| Temp Set Point Range | Internal resistor network | 70 | | 110 | °C |
| | External resistor network | -20 | | 40 | |
| Temp Set Point Resolution | 12-bit resolution | | | 0.04 | °C |

[1] Each internal heater current must be limited to ~175mA continuously for 10yr operational lifetime @ 120C junction temperature

[2] Maximum continuous power output for 10yr operational lifetime @120C junction temperature

## Oscillator Specifications

**Table 4 Oscillator Specifications**

| Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Input Frequency | Internal CA/CB capacitors only | 5[1] | | 155 | MHz |
| CA Range | Adjustable | 2 | | 52 | pF |
| CB Range | Adjustable | 2 | | 62 | pF |
| RD Range | Adjustable | 25 | | 500 | Ω |
| RF Range | Adjustable | 1.6k | | 100k | Ω |
| Duty Cycle | Adjustable | 45 | 50 | 55 | % |
| Phase Noise Floor | 1MHz offset | | -165 | | dBc/Hz |

[1] Using external capacitors allows for operation below 5MHz

## Output Specifications

**Table 5 Output Stage Specifications**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Maximum Output Frequency | 15pF load | | 200 | | MHz |
| | 50pF load | | 100 | | |
| Rise/Fall Time (10%-90%) of VDDA | Fast Slew Rate - 15pF Load | | 2.0 | | ns |
| | Fast Slew Rate - 50pF Load | | 4.8 | | |
| | Slow Slew Rate - 15pF Load | | 3.7 | | |
| | Slow Slew Rate - 50pF Load | | 9.1 | | |

# PIN CONFIGURATION AND FUNCTION

**Table 6 TM200 Pinout**

| Pin | Name | I/O/P | Description |
|---|---|---|---|
| 1 | OSCD | I/O | Crystal drive when internal Varicap is used. |
| 2 | OSCC | I/O | Crystal drive when internal Varicap is bypassed and not used. |
| 3 | VDDH1 | P | 3.3V Internal Heater supply. The current on this pin can be up to 175mA. |
| 4 | BYPASS | I/O | 2.9V Internal regulator compensation. A 1nF capacitor to ground is recommended. This node is the power supply for the internal oscillator. |
| 5 | GNDD | P | Digital ground |
| 6 | SCL | I/O | Tuning (EFC) & $I^2C$ interface input clock. An external pullup resistor to VDDA of 10kΩ is needed during $I^2C$ communications. The pin contains an internal pull-down resistor of 110 kΩ |
| 7 | SDA | I/O | Open drain serial data input/output for the $I^2C$ interface. An external pullup resistor to VDDA of 10kΩ is needed during $I^2C$ communications. The pin contains a high value internal pull-down resistor. |
| 8 | N/C | n/a | Not connected |
| 9 | MUX | I | General purpose input for ADC conversion. Signals on this pin can be sampled, converted to the digital domain, and used as part of the correction/monitoring algorithm. One possible connection is to an external NTC thermistor to measure temperature at a specific location. |
| 10 | XTUNE | I/O | External Tuning Voltage. The pin is driven by the output of the Correction DAC or the EFC input. It typically controls the voltage on a varactor. It is not connected when the Correction block is configured to drive the internal Varicap. |
| 11 | EN | I/O | Enable signal. The polarity and default state is programmable through the internal processor. |
| 12 | HTHRM | I/O | Heater Thermistor Connection |
| 13 | VDDH2 | P | 3.3V Internal Heater supply. The current on this pin can be up to 175mA. |
| 14 | RFOUT | O | RF Output. The RFOUT pin provides a CMOS output signal with properties defined in the output stage section. |
| 15 | RFIN | I | RF Input. RFIN is the input receiver connection from the oscillator stage output. It is usually driven via a capacitor from OSCB. |
| 16 | HDRV | O | External Heater Drive |
| 17 | MUX | I | General purpose input for ADC conversion. Signals on this pin can be sampled, converted to the digital domain, and used as part of the correction/monitoring algorithm. One possible usage would be for measuring a NTC (Negative Temperature Coefficient) thermistor to measure the temperature at a specific location. |
| 18 | VDDA | P | 3.3V Analog positive supply. The current on this pin can be up to 20mA. |
| 19 | OSCB | I/O | Pierce inverter state output. This signal is usually fed to RFIN via a series capacitance to provide a drive to the output stages. |
| 20 | OSCA | I/O | Pierce inverter stage input from crystal. |
| 21 | GNDA | P | Analog ground |

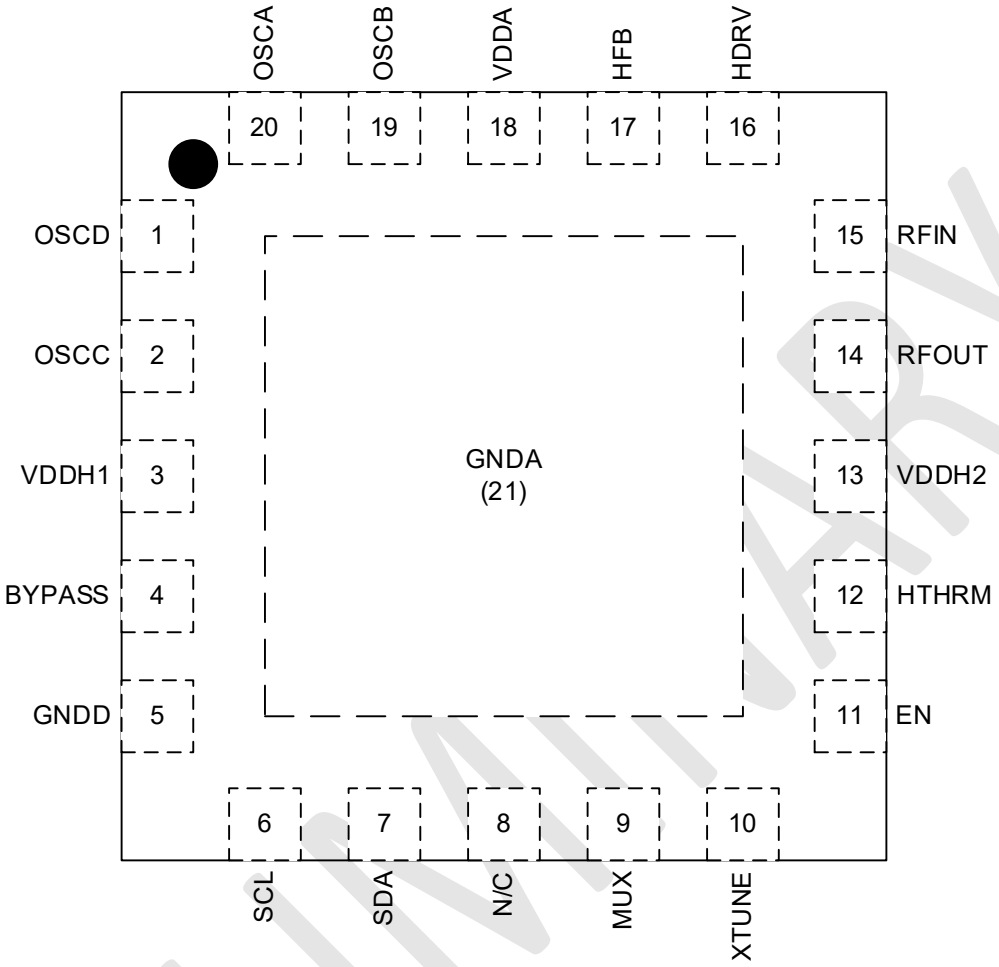



**Figure 1 TM200 Package Pinout**

# BLOCK DESCRIPTION & FUNCTIONALITY

## Oscillator Stage

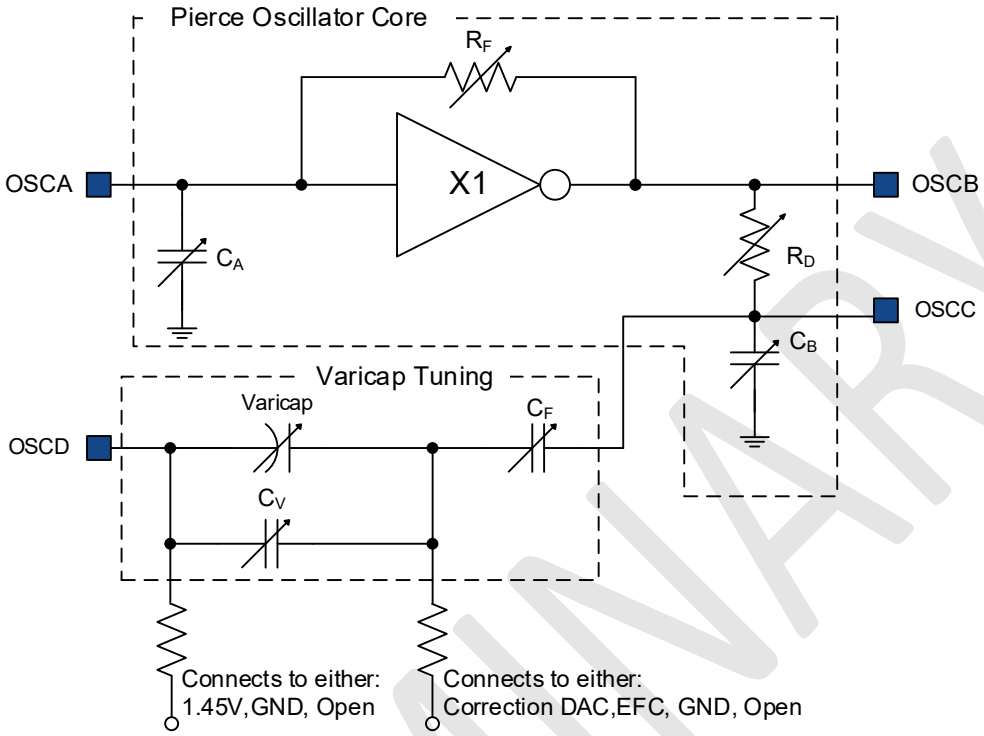



**Figure 2 Oscillator Stage Architecture**

### Pierce Oscillator Core

The oscillator uses a Pierce architecture, designed to be compatible with fundamental or overtone AT cut crystals and overtone SC cut crystals up to 156MHz. It includes an embedded inverter with adjustable resistors and capacitors. The gain stage (X1) is an optimized P/N FET inverter pair. The values for $C_A$, $C_B$, $C_F$, $C_V$, $R_F$, and $R_D$ are set using the control registers. The oscillator stage is powered from an internally regulated 2.9V supply or from an external regulator for high performance applications through the BYPASS pin.

Most oscillator applications can be met with the internal components. The $R_F$ and $R_D$ select logic allows disabling the internal resistors for use with external components. $C_A$ and $C_B$ capacitors can be fully disabled especially for applications with matching and trap networks in series with overtone crystals.

Four digital bits control the $C_A$ value. When all bits are off, the minimum capacitance is ~2pF. The bit 0 value is 5pF, bit 1 is 10pF, bit 2 is 15pF, and bit 3 is 20pF. $C_B$ works in a similar manner except bit 3 is 30pF.

### Varicap Tuning

The Varicap, $C_V$, and $C_F$ provide internal voltage controlled tunability. The Varicap capacitance varies with the DC voltage applied via the two control points shown in the diagram. $C_V$ controls the capacitance range of the Varicap. $C_F$ is a series capacitor that can also tune the Varicap operation.

In Figure 2, the Varicap capacitance is 9pF when the voltage applied to the right-hand terminal is 2.9V and the left-hand terminal is 1.45V. When the right-hand terminal is 0V and the left-hand terminal is 1.45V, the capacitance is 34pF.

**Oscillator Connections**

OSCA is the Pierce inverter input, typically connected to one side of the crystal. OSCB is the Pierce inverter output used to feed the TM200 output stage. For applications that use an external varactor, the other side of the crystal is connected to OSCC and OSCD is left open.

OSCA and OSCD are the crystal connections for applications that use the internal Varicap. A blocking cap is necessary between OSCD and the crystal to prevent DC bias across the crystal.

## RF Output Stage

The RF Output Stage block conditions the final RF output waveform of the oscillator signal, usually driven by a capacitor from OSCB. It restores the clock edges, makes duty cycle adjustments, and performs any necessary clock division before driving the output load. The block also detects the presence or absence of an oscillator input signal and buffers the clock signal for use as a microprocessor clock.

Clock frequency divisions of 1, 2, 4 and 8 are available. The CMOS clock driver has a low/high slew rate setting that allows the user to select the appropriate drive characteristics for a given output load.

An enable function under the control of the MCU allows the output to go tri-state.

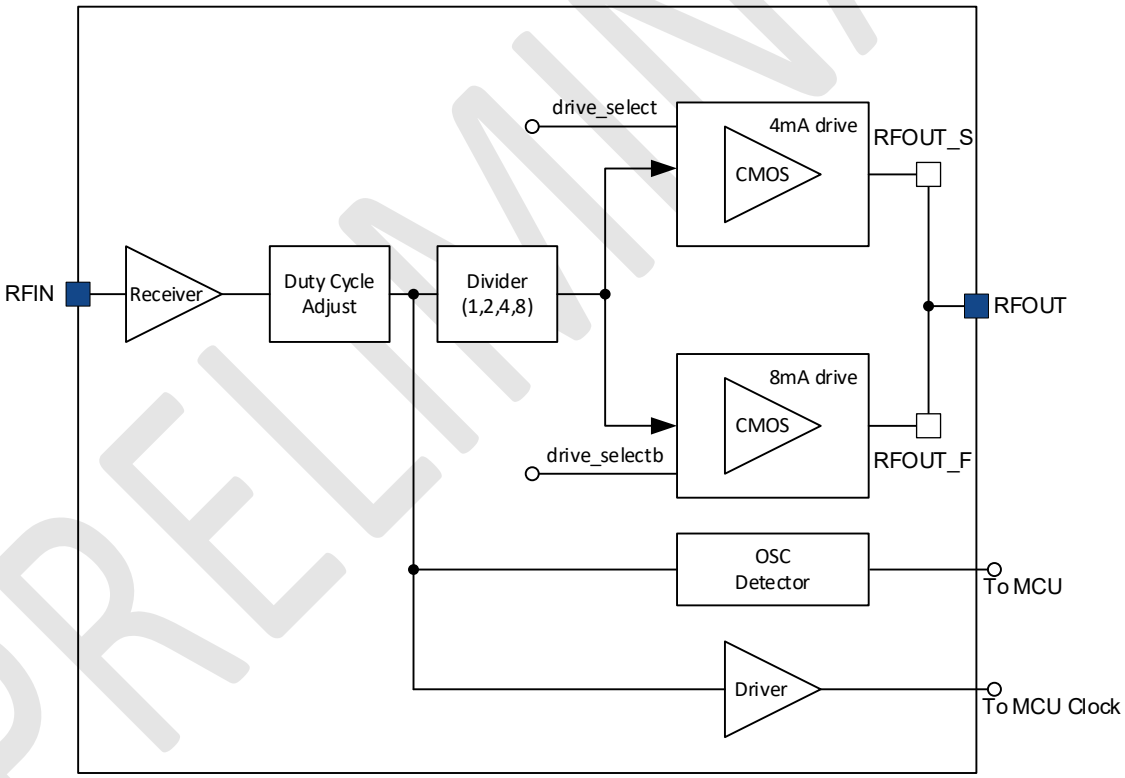



**Figure 3 RF Output Stage Architecture**

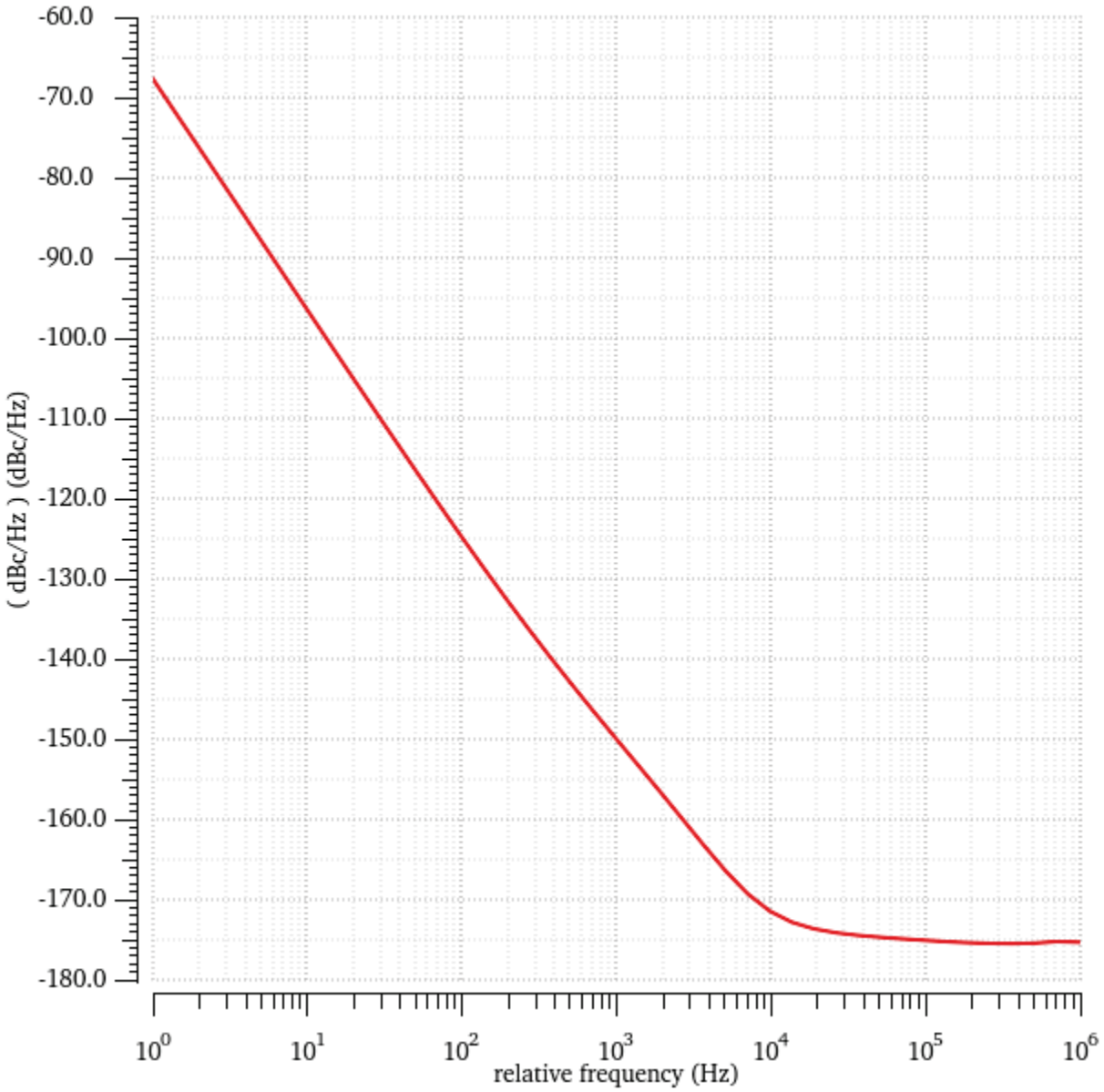



**Figure 4 - 20MHz Fundamental, AT-Cut, Internal Varicap Phase Noise**

## Correction

The Correction block is used to trim the frequency shifts of the crystal across temperature (Beckman Curve) through either the TM200's internal Varicap or an external varactor. Using the ADC to provide temperature sensor data, the MCU provides the input code to a 12-bit DAC with an output voltage that adjusts the Varicap (or external varactor) and correct crystal frequency variation across temperature.

The correction block uses either the internal Varicap or an external varactor to provide the appropriate crystal pull. The internal Varicap is suitable for low-cost designs that require minimal components. For higher performance requirements, an external varactor can be used and controlled with the XTUNE pin. Please refer to the OCXO Design Examples for more information.

The internal Varicap or XTUNE pin can also be controlled from the dual use SCL (EFC) pin via an analog connection. Alternately the EFC, MUX0, or MUX1 pin can be used as an input to the ADC. The digitized value is processed in the MCU via correction algorithms and fed out via the correction DAC to control the Varicap or external varactor.

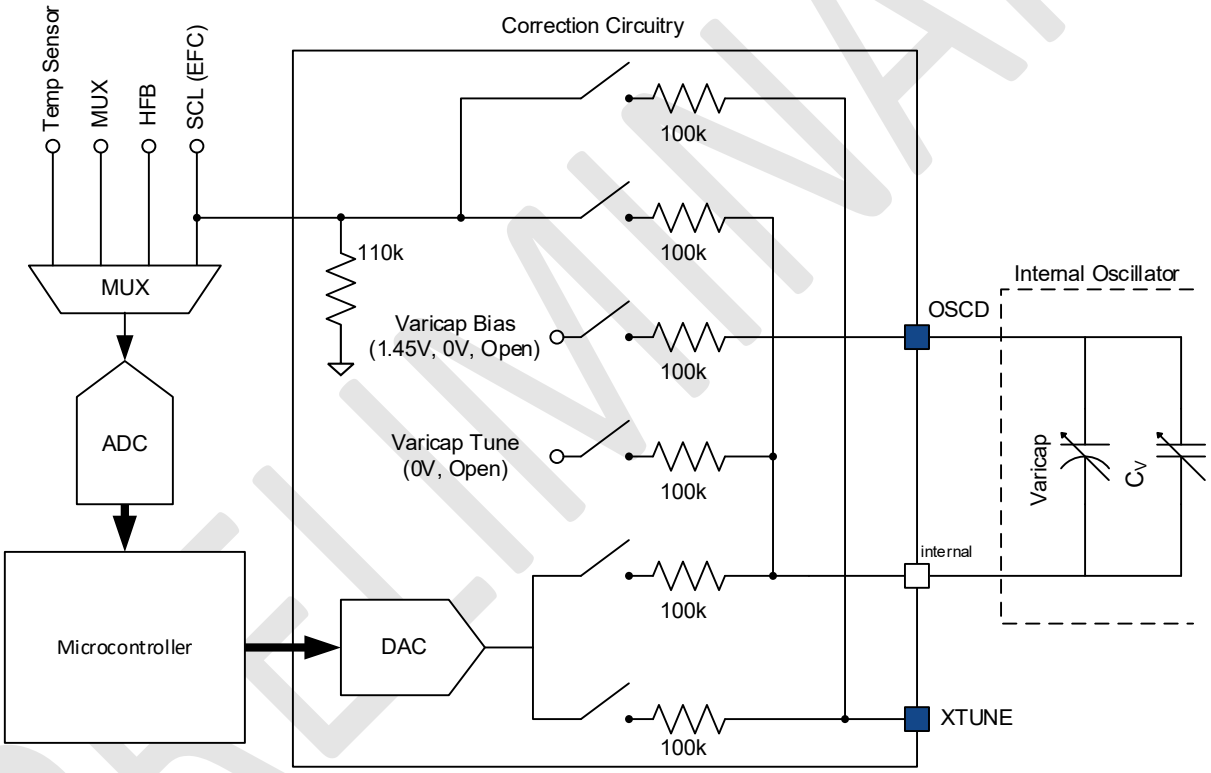



**Figure 5 Correction Block Diagram**

## Internal Heater

Two nominal 0.565W heating elements are used to produce a minimum 1W of total output power at -40 degrees with a 3.3V supply. The heating elements are placed to provide excellent thermal uniformity. The heaters are composed of NMOS FET devices in source follower configurations with a resistive load as the heating element. With an NMOS architecture, the HFB terminal swings roughly between 0V to 0.7V as the HDRV terminal swings between 0V to 3.3V.

HDRV and HFB are controlled and sensed, respectively, by the Thermal Controller and no external connections to those pins are necessary. In the case where more than 1W of power output is desired, external heater elements can be used and controlled to the Thermal Controller through HDRV and HFB. The use of internal and external heaters at the same time is not supported as the Thermal Controller is only capable of stabilizing one thermal loop. Multiple instances of the IC can be used to support independent functions.

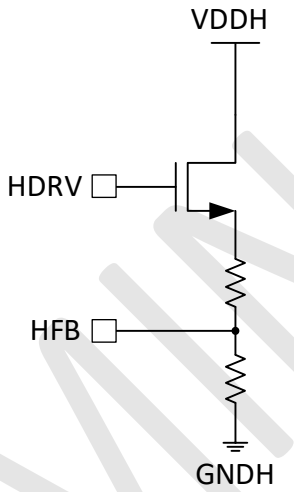



**Figure 6 Basic Heater Structure**

## Thermal Controller

The Thermal Controller is used to control the thermal characteristics of the module being constructed. The controller uses a heater driver to control transistors with resistive loads to dissipate power and cause the cavity temperature to rise. An external thermistor provides data input into the feedback network to adjust and stabilize the cavity temperature. The controller achieves low Allan deviation (ADEV) with a low noise circuit design. The Thermal Controller can be used as a simple temperature feedback loop or dynamically adjusted using the Temperature Set DAC controlled by an MCU program.

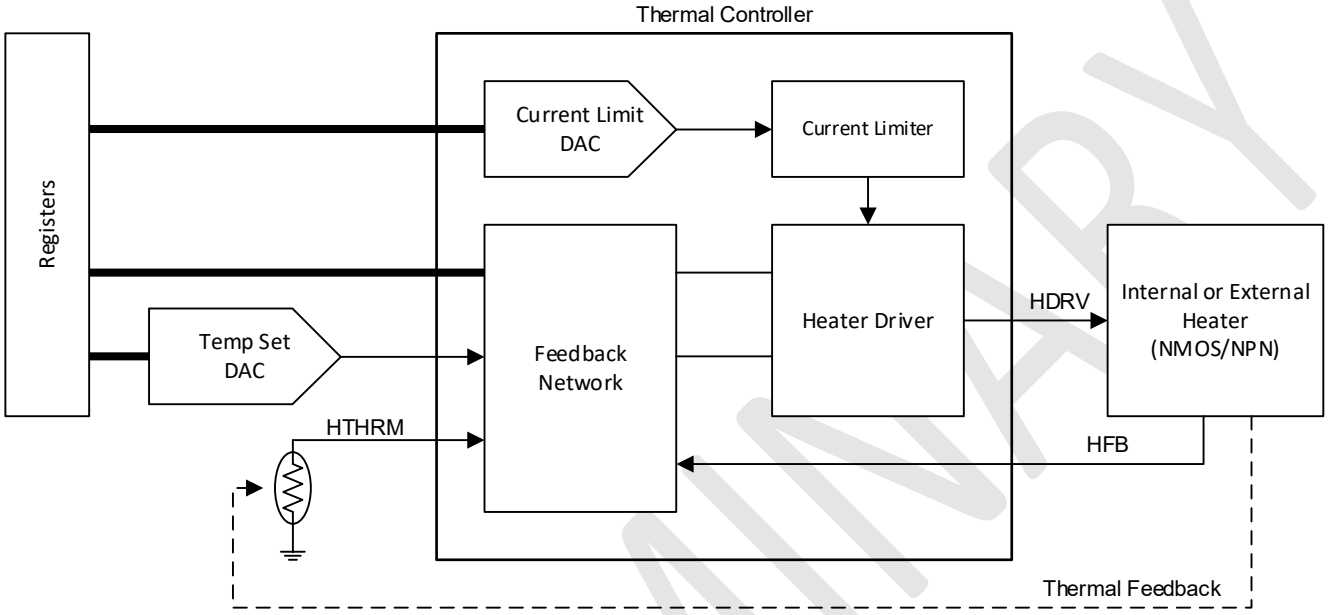



**Figure 7 Thermal Controller**

### Temperature Set Point

Two elements set the controller's settling temperature. First, the value of a coarse temp set resistor located in the feedback network is adjusted to coarsely to match the temperature range segment in the 70 to 110 C range and thermistor (100kΩ NTC) curve. When the internal logic for the coarse temperature set resistor is "open", an external resistor allows finer grained control of the temperature curve as needed. Second, the 12-bit Temp Set DAC provides an additional current up to 50-100µA provides additional fine temperature setting. This will provide a resolution of <0.039°C. The Temp Set DAC also allows for thermal coupling and resonator characteristics.

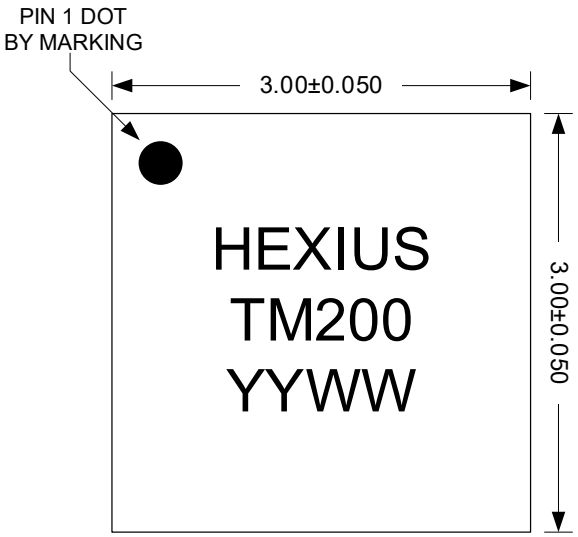
### Loop Dynamics

The loop is stable with excellent phase margin based on the internal compensation network. The internal compensation assumes current feedback in addition to thermal feedback. No external components are needed. Controlling the internal heaters in conjunction with external heaters is not supported as the loop stability dynamics can be significantly different. This is especially the case between NMOS and NPN transistors.

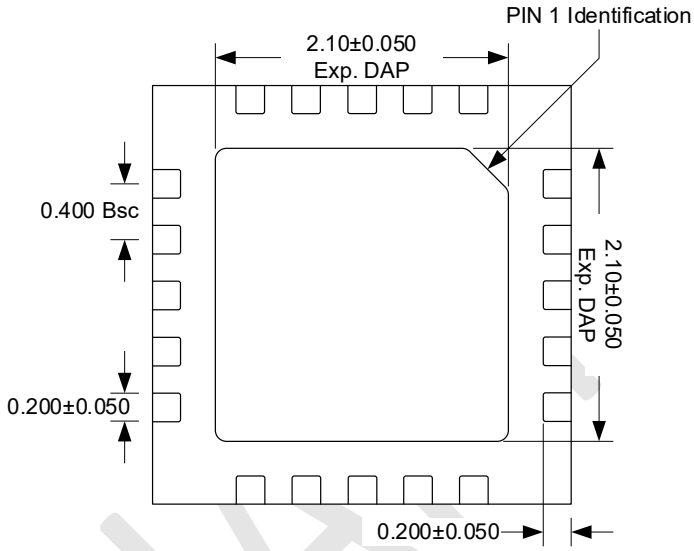
### MCU Thermal Controller Inputs

The HFB, HTHRM, and internal temperature sensor signals are digitized under program control and fed to the MCU through the common ADC. The resulting data is used for diagnostics, algorithm adjustments, and related purposes.

## PACKAGE OUTLINE




TOP VIEW

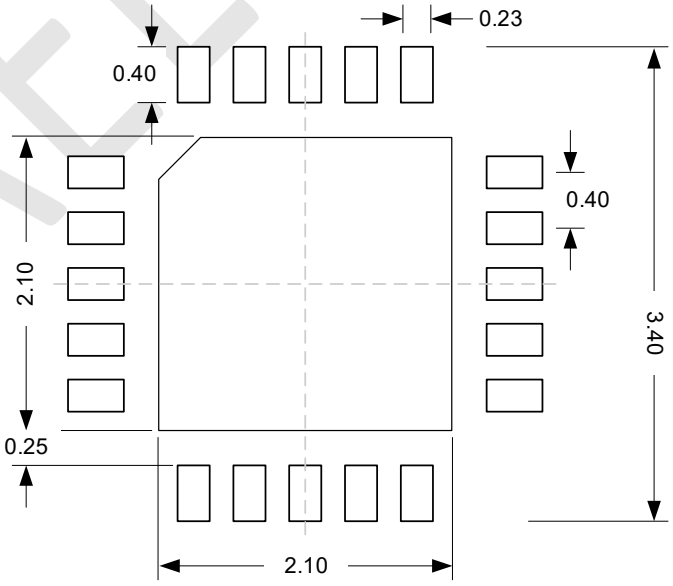



BOTTOM VIEW

*All units are in millimeters*


SIDE VIEW

### PCB LAND PATTERN/FOOTPRINT



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