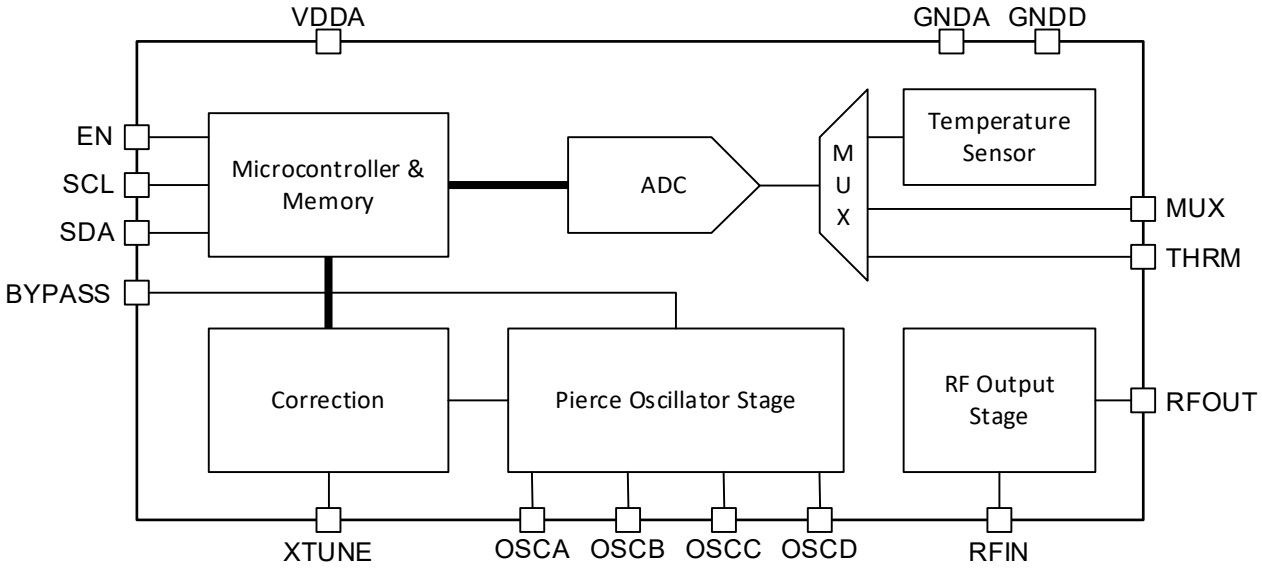
TCXO Thermal Management IC

DESCRIPTION

The TM100 is a fully integrated programmable thermal management unit that monitors, controls, and corrects analog circuitry across a wide temperature range. The TM100 is primarily intended for TCXO applications and includes a temperature sensor, internal Pierce oscillator & output stage and data converters combined with a microcontroller (MCU) and memory structures to run temperature correction programs. The integrated Pierce oscillator and output stage are designed to be flexible with a variety of oscillator and crystal configurations. The TM100 includes many programmable functionality options, and a software package makes it easy to configure and implement customizable crystal correction algorithms. It communicates via an I^2C interface and is available in a 3mm x 3mm package or as die.

BLOCK DIAGRAM



FEATURES

- Low Phase Noise Oscillator
- High accuracy temperature sensor
- Various crystal correction options available
  - Selectable Polynomial Order Curve-Fit
  - Linear Lookup Table
  - < 25ppb frequency stability
- Software configuration

APPLICATIONS

- TCXO Modules

ORDERING INFORMATION

Order Number	Package	Quantity	RoHS	MSL Rating	Leadframe
TM100-T1	20L STSLP QFN	122 – Tube	Yes	1	NiPdAu
TM100-R1	20L STSLP QFN	1000 – Reel	Yes	1	NiPdAu
TM100-X	Die	Upon Request	n/a	n/a	n/a

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REVISION HISTORY

Revision	Date	Description
1.0	01/2023	Initial Release
1.1	06/2023	Corrections

SPECIFICATIONS

Environmental Specifications

Table 1 Recommended Operating Conditions

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage	± 5%	3.135	3.3	3.465	V
Operating Temperature		-40		125	°C
OTP Programming Temperature		0		50	°C

Internal Temperature Sensor Specifications

Table 2 Internal Temperature Sensor Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Absolute Accuracy		-0.25		0.25	°C
Voltage Range	-40C to 125C	1.32		2.5	V
Resolution	ADC LSB		0.11		°C
Linearity	-40C to 125C		0.6		%
	70C to 125C		0.2		

Data Converter Specifications

Table 3 Correction DAC DC Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Temperature Range		-40	27	125	°C
Monotonicity		12			Bits
Resolution		12			Bits
Least Significant Bit	BYPASS = 2.9V		0.708		mV
Differential Non-Linearity		-1	±0.5	+1	LSB
Integral Non-Linearity		-4	± 2	+4	LSB
Output Range	BYPASS = 2.9V	0.3		2.9	V

Oscillator Specifications

Table 4 Oscillator Specifications

Description	Conditions	Min	Typ	Max	Unit
Input Frequency	Internal CA/CB capacitors only	5[1]		155	MHz
CA Range	Adjustable	2		52	pF
CB Range	Adjustable	2		62	pF
RD Range	Adjustable	25		1000	Ω
RF Range	Adjustable	1.6k		100k	Ω
Duty Cycle	Adjustable	45	50	55	%

[1] Using external capacitors allows for operation below 5MHz

Output Specifications

Table 5 Output Stage Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Maximum Output Frequency	15pF load		200		MHz
	50pF load		100		
Rise/Fall Time (10%-90%) of VDDA	8mA drive - 15pF Load		2.0		ns
	8mA drive - 50pF Load		4.8		
	4mA drive - 15pF Load		3.7		
	4mA drive - 50pF Load		9.1		

Digital Clock Specifications

Table 6 Processor Clock Frequency

Parameter	Conditions	Min	Typ	Max	Unit
Internal Ring Oscillator Frequency			10		MHz
Processor Clock Frequency		1		10	MHz
OTP Read Temperature		-40		125	°C
OTP Programming Temperature	Set VDDA to 3.465V for best results	0		50	°C
OTP Memory Size			32k		Bytes
ROM Memory Size			3k		Bytes
RAM Memory Size			1k		Bytes

Absolute Maximum Ratings

Table 7 Absolute Maximum Ratings

Parameter	Conditions	Min	Max	Unit
Supply Voltage		0.5	3.8	V
Pin Voltage	EN	-0.5	5.5	V
	SCL	-0.5	5.5	
	SDA	-0.5	5.5	
	All Other Pins	-0.5	3.8	
Soldering Temperature			260	°C
Storage Temperature		-55	150	°C
Junction Temperature			150	°C
ESD Ratings	Human Body Model (HBM)	2000		V
	Machine Model (MM)	100		
	Charged Device Model (CDM)	1000		

PIN CONFIGURATION AND FUNCTION

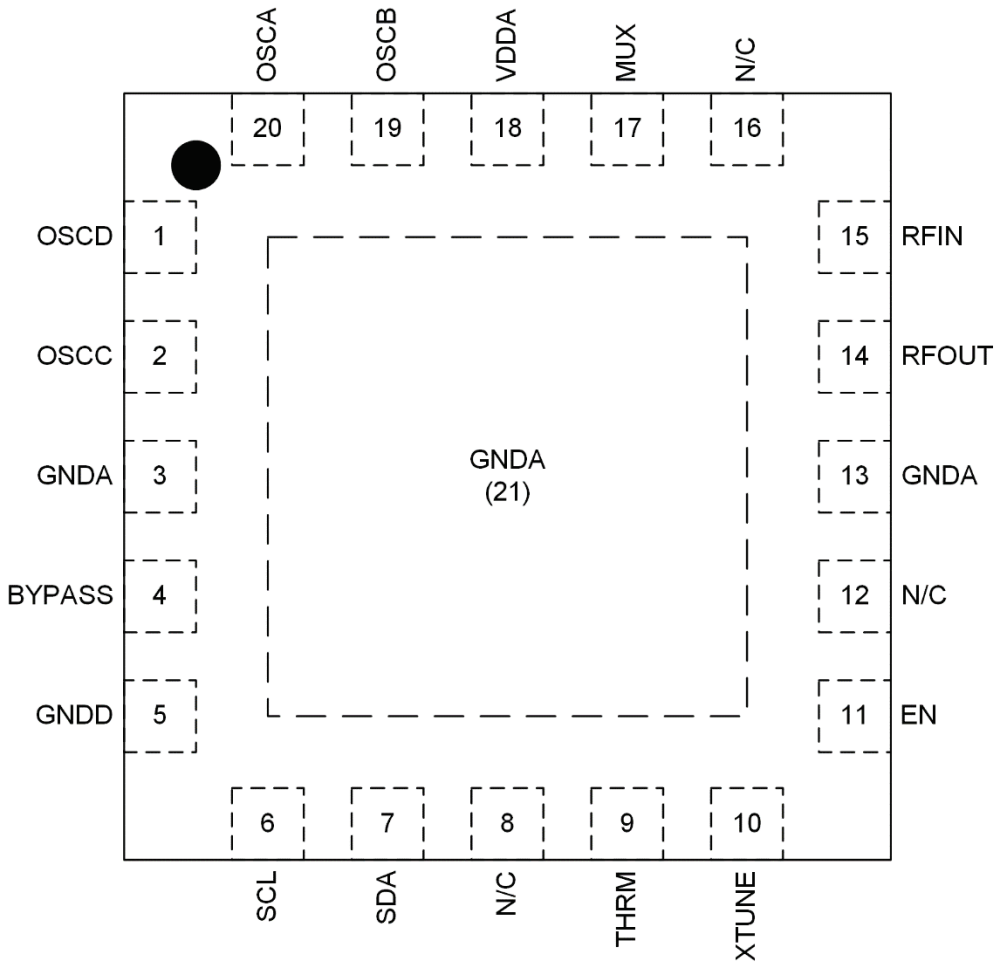


Figure 1 TM100 Package Pinout

Table 8 TM100 Pinout

Pin	Name	I/O/P	Description
1	OSCD	I/O	Crystal drive when internal Varicap is used.
2	OSCC	I/O	Crystal drive when internal Varicap is bypassed and not used.
3	GNDA	P	Analog ground
4	BYPASS	I/O	Internal oscillator power supply. Will require either 22uF/0.01uF bypass capacitors or 1nF compensation capacitor depending on configuration.
5	GNDD	P	Digital ground
6	SCL	I/O	Tuning (EFC) & I^2C interface input clock. An external pullup resistor to VDDA of 10kΩ is needed during I^2C communications. The pin contains an internal pull-down resistor of 110kΩ. 5V tolerant.
7	SDA	I/O	Open drain serial data input/output for the I^2C interface. An external pullup resistor to VDDA of 10kΩ is needed during I^2C communications. The pin contains a high value internal pull-down resistor. 5V tolerant.
8	N/C	n/a	Not connected
9	THRM	I	External NTC thermistor input. Use this input to use an external thermistor as an alternative crystal measurement method than the internal IC temperature sensor.
10	XTUNE	I/O	External Tuning Voltage. The pin is driven by the output of the Correction DAC and/or the EFC input. It typically controls the voltage on an external varactor. It is not connected when the Correction block is configured to drive the internal Varicap.
11	EN	I/O	Enable signal. The polarity and default state is programmable through the internal processor. 5V tolerant.
12	N/C	n/a	Not connected
13	GNDA	P	Analog ground
14	RFOUT	O	RF Output. The RFOUT pin provides a CMOS output signal with properties defined in the output stage section.
15	RFIN	I	RF Input. RFIN is the input receiver connection from the oscillator stage output. It is usually driven via a capacitor from OSCB.
16	N/C	n/a	Not connected
17	MUX	I	General purpose input for ADC conversion. Signals on this pin can be sampled, converted to the digital domain, and used as part of the correction/monitoring algorithm. Contact Hexius for use of this pin.
18	VDDA	P	3.3V Analog positive supply. The current on this pin can be up to 20mA.
19	OSCB	I/O	Pierce inverter state output. This signal is usually fed to RFIN via a series capacitance to provide a drive to the output stages.
20	OSCA	I/O	Pierce inverter stage input from crystal.
21	GNDA	P	Analog ground

BLOCK DESCRIPTION & FUNCTIONALITY

Oscillator Stage

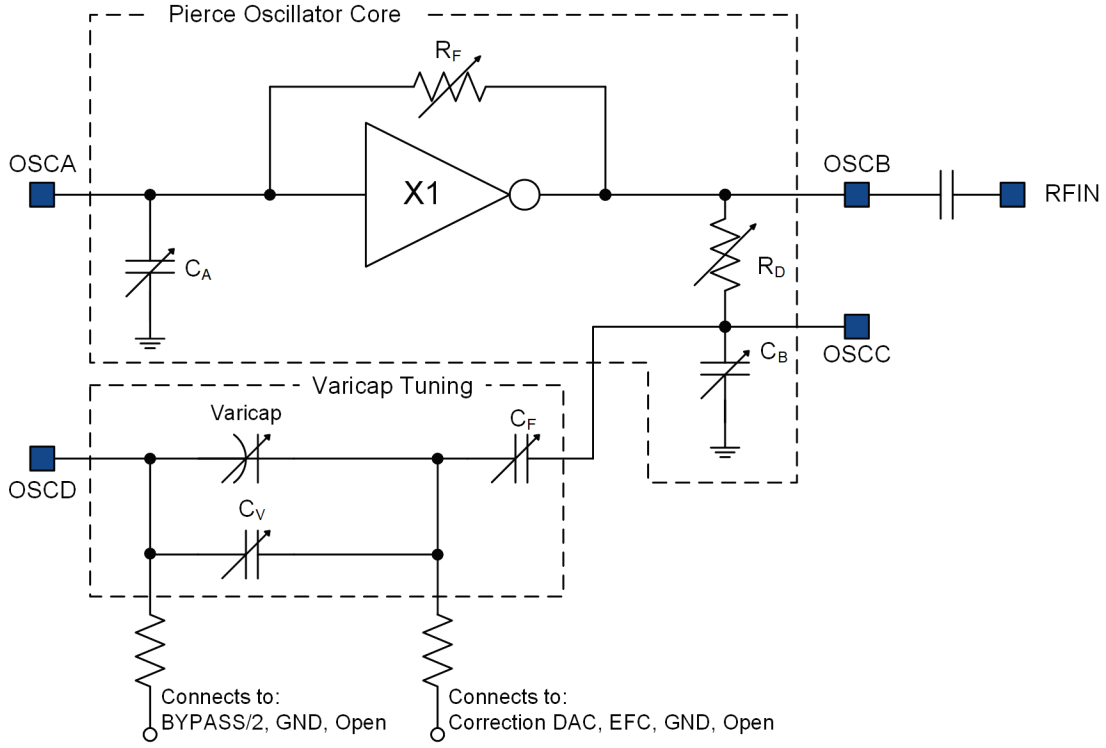


Figure 2 Oscillator Stage Architecture

Pierce Oscillator Core

The oscillator uses a Pierce architecture, designed to be compatible with fundamental or overtone AT cut crystals and overtone SC cut crystals up to 156MHz. It includes an embedded inverter with adjustable resistors and capacitors. The gain stage (X1) is an optimized P/N FET inverter pair. The values for C_A, C_B, C_F, C_V, R_F, and R_D are set using the control registers and are easily configured with the TMx00 Control Software. The oscillator stage is powered through the BYPASS pin and can be shorted to the VDDA pin of the IC or decoupled from VDDA by configuring an internal 2.9V regulator to drive the BYPASS pin. See the Application Notes for more information.

Most oscillator applications can be met with the internal component value selections, thereby reducing the amount external components needed to construct an oscillator. Alternatively, the R_F and R_D select logic allows disabling the internal resistors for use with external components. C_A and C_B capacitors can be fully disabled especially for applications with matching and trap networks in series with overtone crystals. When the C_A and C_B capacitors are disabled, the minimum capacitance is ~2pF.

Oscillator Connections

OSCA is the Pierce inverter input, typically connected to one side of the crystal. OSCB is the Pierce inverter output used to feed an output stage. OSCA and OSCD are the crystal connections for applications that use the internal Varicap. A blocking cap may be necessary between OSCC or OSCD and the crystal to prevent DC bias across the crystal. For applications that use an external varactor, the other side of the crystal is connected to OSCC and OSCD is left open.

Please refer to the *TMx00 Design Example Manual* for examples of various oscillator architectures that can be built with the TM100.

Internal Varicap Tuning

The internal Varicap, C_V, and C_F provide internal voltage controlled tunability. The internal Varicap is a MOS device that has a variable capacitance value that varies with the DC voltage applied via the two control points shown in Figure 2. C_V controls the capacitance range of the Varicap. C_F is a series capacitor that can also tune the Varicap operation.

The Internal Varicap capacitance can be varied between 9pF to 34pF depending on the bias condition across the device. Referring to Figure 2, the left-hand terminal of the Varicap is set to the BYPASS/2 voltage when in operation (A GND or OPEN connection is made when an external varactor is used). The right-hand side of the Varicap can be driven from the Correction DAC or EFC pin (A GND or OPEN connection is made when an external varactor is used).

When the voltage applied to the right-hand terminal is at BYPASS voltage, the Varicap capacitance is set to the minimum value of 9pF. Conversely, when the right-hand terminal is 0V, the Varicap capacitance is set to the maximum value of 34pF.

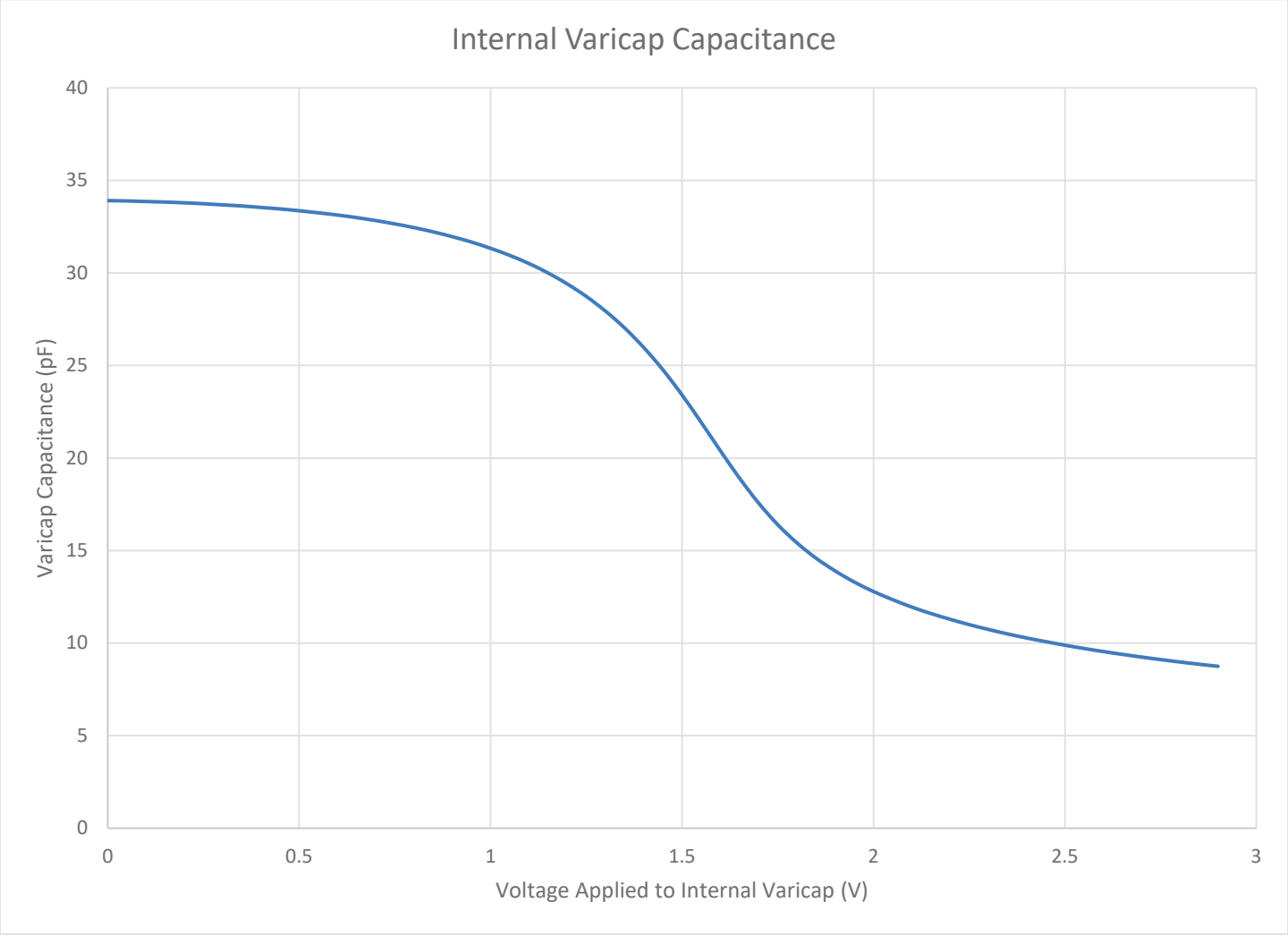


Figure 3 Internal Varicap Capacitance Curve

RF Output Stage

The TM100 includes an RF Output Stage block that conditions the RF output waveform of the oscillator signal, usually driven by a capacitor from OSCB. It restores the clock edges, makes duty cycle adjustments, and performs any necessary clock division before driving the output load. The block also detects the presence or absence of an oscillator input signal (RFIN) and buffers the clock signal for use as an internal microprocessor clock.

Clock frequency divisions of 1, 2, 4 and 8 are available. The CMOS clock driver has a 4mA/8mA drive current setting that allows the user to select the appropriate drive characteristics for a given output load.

An enable function under the control of the MCU allows tri-state output.

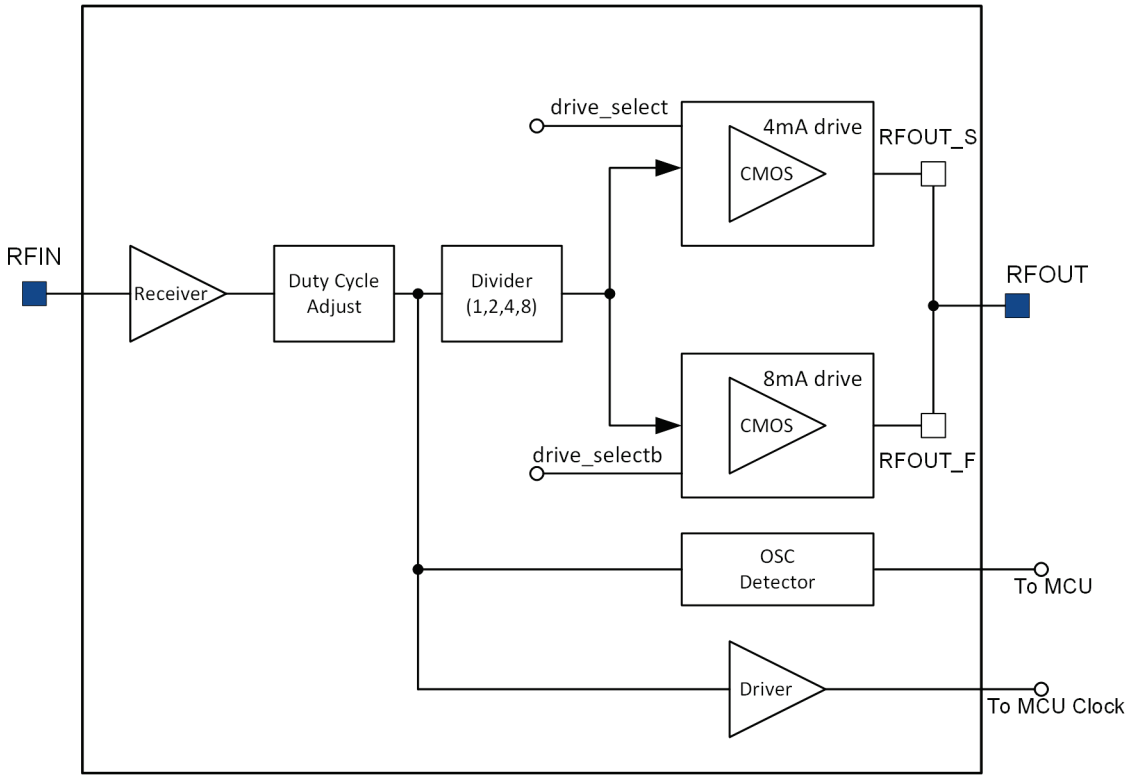


Figure 4 RF Output Stage Architecture

Using the RF Output Stage is not required to produce an output waveform. An unbuffered inverter driven from RFIN is an alternative signal path that may produce a lower phase noise floor. Additional information regarding the output signal generation is described in the Application Notes section.

Correction System

The correction system is designed to correct the frequency shifts of a crystal across temperature (Beckman Curve) with either the TM100's internal Varicap or an external varactor. Using the ADC to convert temperature sensor data, the MCU provides the input code to a 12-bit DAC with an output voltage that adjusts the internal Varicap or external varactor to correct crystal frequency variation across temperature.

The correction system uses either the internal Varicap or an external varactor to provide the appropriate crystal pull. The internal Varicap is suitable for low-cost designs that require minimal components. For higher performance requirements, an external varactor may be used and controlled with the XTUNE pin. Please refer to the *TMx00 Design Example Manual* for architecture examples.

The internal Varicap or XTUNE pin can also be controlled from the dual use SCL (EFC) pin via an analog connection. Alternately the EFC or MUX pin can be used as an input to the ADC. The digitized value is processed in the MCU via correction algorithms and fed out via the correction DAC to control the internal Varicap or external varactor.

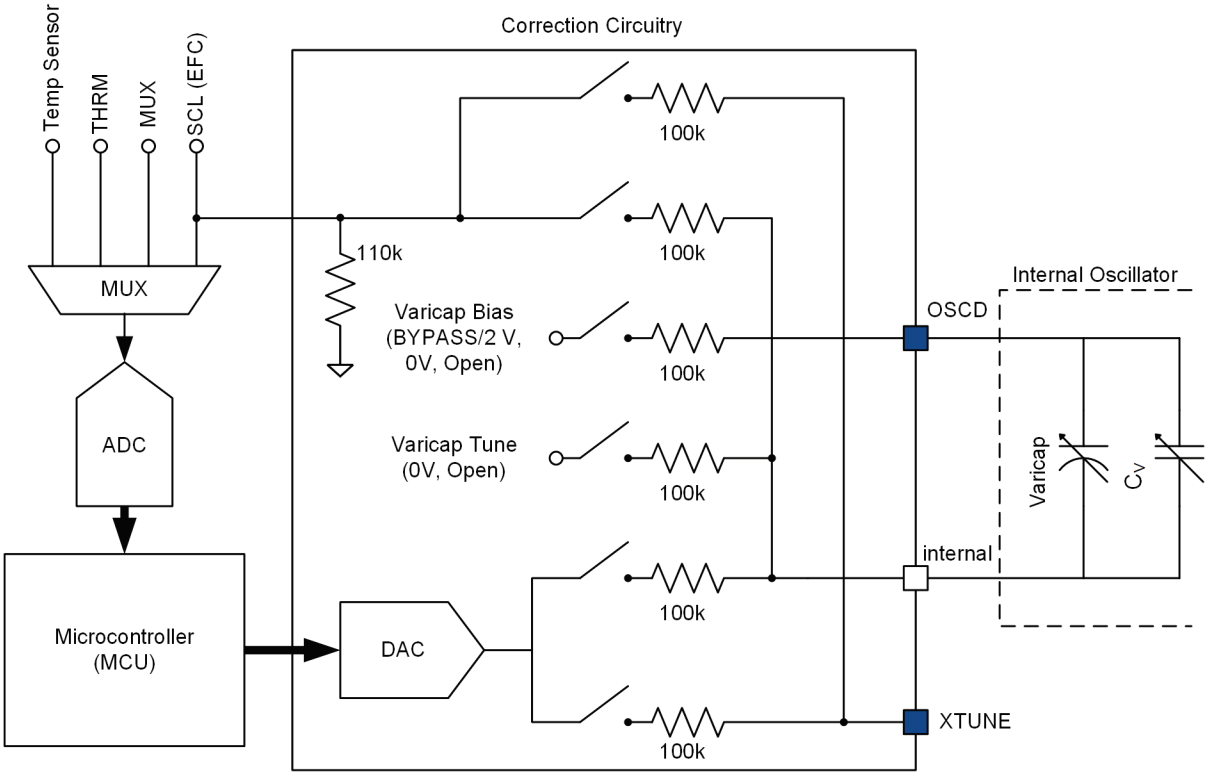


Figure 5 Correction System Diagram

Internal Temperature Sensor

The internal temperature sensor is sampled and digitized by the ADC to provide a 12-bit resolution temperature measurement of the IC. *The measured value is the temperature of the IC substrate*. This value is an indicator of the oscillator crystal temperature with proper module construction. Alternatively, an external thermistor (through the THRM pin) can be used for temperature measurements, correction, and monitoring. The internal temperature sensor is located near the center of the die and is calibrated during production test. Reference Design Examples and Application Notes for more information about thermal coupling.

Analog to Digital Converter & MUX

The ADC is a Successive Approximation architecture (SAR) in combination with a multi-channel input MUX. This architecture provides medium conversion speed and digitizes certain internal signals required to implement the correction algorithm. Control of the ADC and MUX is self-contained within the TM100 software. THRM and MUX pins are available for additional external temperature measurements and other signal monitoring functions. Please reference the Application Notes for more information about using the THRM and MUX inputs.

Power Domains

The TM100 operates with the following external voltage domains:

- VDDA - 3.3V Main analog supply
  - Required supply voltage
- BYPASS – Internal Oscillator Supply (connection options listed below)
  - Shorted to VDDA
  - Internal 2.9V Regulator
  - External regulator

Upon application of VDDA power, the POR (Power on Reset)/Power Sequencing block enables the bandgap and 1.8V regulator. Other internal regulators startup with the proper delays defined within the IC. The timing control and power sequencing ensures the MCU, memory, and analog blocks start up in the correct sequence. The POR structure and startup sequencing makes the IC tolerant to wide variations in supply rise time up to 1sec. If the internal 2.9V BYPASS regulator is enabled, a 1nF capacitor on the BYPASS pin to ground is required for stability.

The BYPASS pin (oscillator supply) has 3 connection options. The first is to short it to VDDA. Alternately, the oscillator supply can be decoupled from VDDA and driven with the Internal 2.9V Regulator. Lastly, the BYPASS pin can be driven by a separate external regulator. Further information is available in the Application Notes.

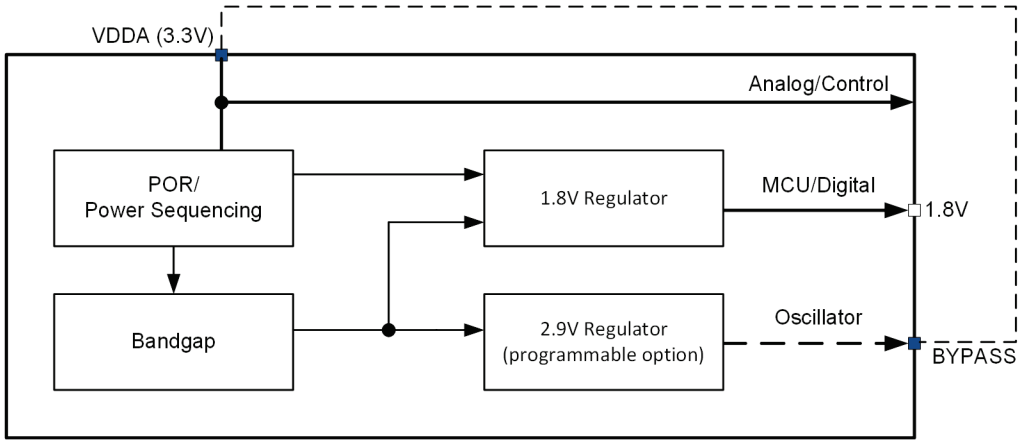


Figure 6 Supply and Voltage Domains

Microcontroller & Memory

The control unit for the IC is an embedded 8-bit microcontroller (MCU) including ROM, RAM, and OTP programmable memory. The microcontroller's main purpose is to configure, store, and adjust parameters. The embedded firmware actively tunes the crystal based on the sensed temperature.

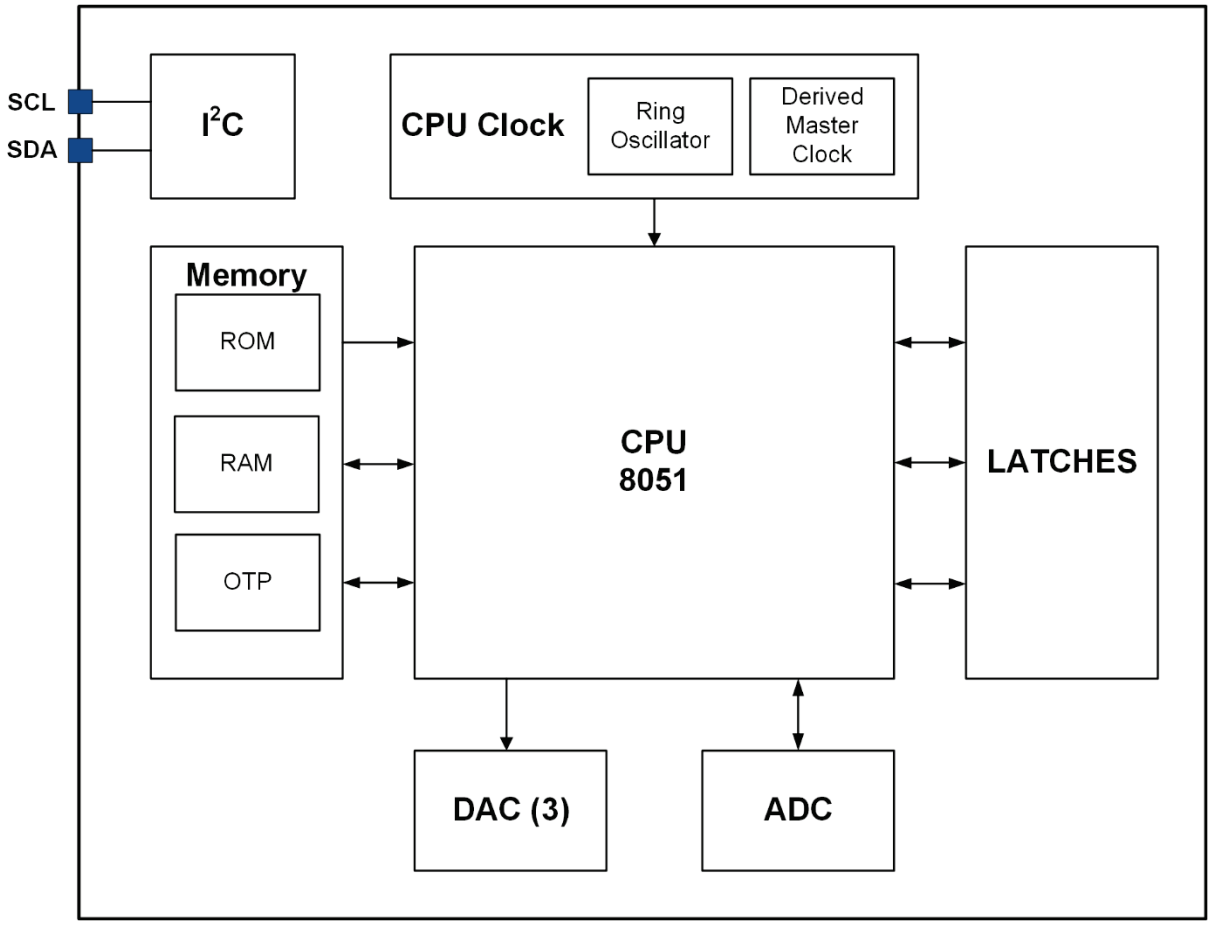


Figure 7 Digital Architecture

1. *I²C Communications*

Setup of the TM100 is supported via the I²C interface. Refer to *TMx00 Programming Reference Manual* for details of the commands.

Table 9 TM100 Communication Interface

TM100 Communication Interface	
Interface Type	I²C Slave 3.3V open drain external pullups required < 10kΩ when active
Max Data Rate	100kbps
Address	5A hex
Data Pin	SDA
Clock Pin	SCL

2. *Programmable Memory*

The nonvolatile programmable memory (OTP) allows customers to store TM100 setup items including oscillator setup, TCXO frequency corrections over temperature, production serial numbers/trackability information, and other items as needed.

Typically, test sequences and program code will be programmed into the OTP memory during Hexius' production test. For customer production flows, the specific customer parameters for operational modes and oscillator configuration are initially loaded into RAM during the testing and burn-in phase. When those parameters are determined to be stable, commands issued to the microcontroller via the I^2C interface write the resulting setup parameters into the nonvolatile OTP memory. Each time power is applied to the TM100, the contents of the nonvolatile OTP memory are used to configure the IC to the desired state.

Each OTP memory location can only be written one time. However, the OTP memory contains several subsections which allow effectively multiple rewrites (6) of the setup parameters, allowing rework and fine adjustment after burn-in and aging test cycles.

The OTP memory has a read temperature range of -40C to +125C, with a programming temperature range of 0C to 50C. For best programming results when writing OTP code sets, the VDDA supply voltage should be set to the maximum value, 3.465V.

Microcontroller Clock Source

No external clock source is required for the microcontroller. At power on reset, an internal self-starting clock of nominally 10MHz (ring oscillator) provides the master clock to the microcontroller. Under software control, the microcontroller clock source can be switched glitch-free from the ring oscillator to a signal from the crystal oscillator. Operating the microcontroller from the crystal oscillator will likely result in lower noise spurs from a common clock source. The microcontroller target clock speed is between 1 and 10 MHz, and internal frequency dividers provide the proper clock rate for TCXO outputs exceeding 10MHz.

A detector circuit determines if a stable oscillator operation is available. The processor reads a flag from the detector circuit and controls the switch to the main oscillator as commanded by software. If the main oscillator fails, the µP will automatically switch back over to the internal ring oscillator.

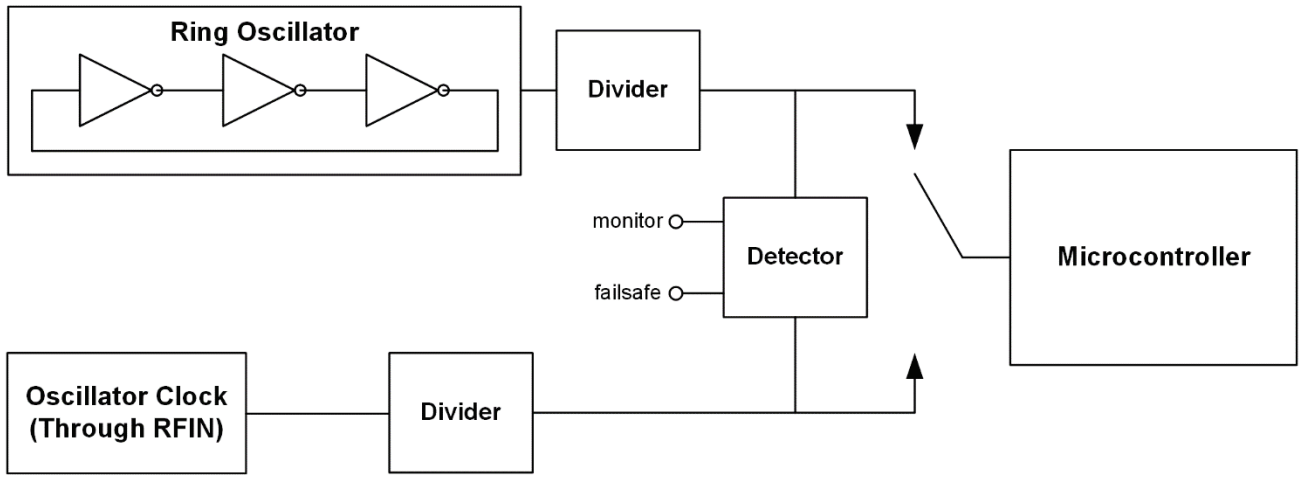


Figure 8 Clock Source Switching

TCXO TEMPERATURE CORRECTION ALGORITHM OVERVIEW

The TM100 supports three correction algorithms to compensate for temperature and voltage non-idealities:

1. **Lookup Table** – Temperature correction algorithm
2. **Temperature Polynomial Curve Fit** – Temperature correction algorithm
3. **Supply Voltage Curve Fit** – Voltage correction algorithm

The TMx00 correction algorithms use integer numbers (digital codes) that represent temperatures and voltages to make compensation adjustments. The ADC converts analog signals into the digital domain for the MCU to calculate the appropriate Correction DAC input code and produce an analog correction voltage.

The first two algorithms use a *Temp Code* input to generate a *CorrDAC Code* from the Correction DAC output to correct frequency variations over temperature. Only one of the temperature correction algorithms may be used during operation.

The *Temp Code* value is an integer with the range of 0 to 4095 and corresponds to the temperature being measured and digitized through the ADC. A -40C to 90C temperature range will utilize a *Temp Code* range of approximately 2000 to 3200. The *Temp Code* is produced from either the IC internal temperature sensor or an external thermistor (via the THRM pin).

The *CorrDAC Code* value is an integer with the range of 0 to 4095 and corresponds to the DAC input code needed to vary the capacitance across an external varactor or the internal TMx00 Varicap to correct the frequency variation for a given temperature.

The *CorrDAC Voltage* is resulting Correction DAC output voltage for a given *CorrDAC Code*. It is calculated by multiplying the Correction DAC's reference voltage by the ratio of the *CorrDAC Code* to the Correction DAC's full-scale code (4095).

$$CorrDAC\ Voltage = \frac{CorrDAC\ Code}{4095} * BYPASS\ Pin\ Voltage$$

As a brief relationship example, a measured temperature of 25C may produce a *Temp Code* of 2541 and results in a *CorrDAC Code* of 1983 and a *CorrDAC Voltage* of 1.4043V for the correct center frequency of a unique TCXO assembly.

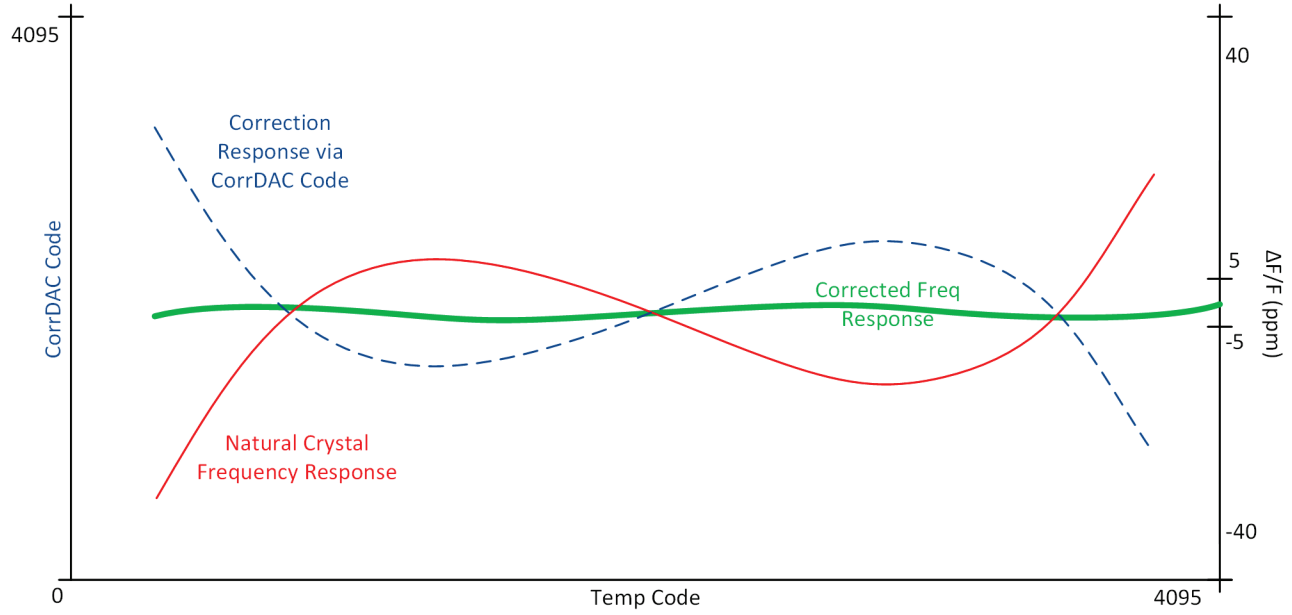


Figure 9 Temp Code and CorrDac Code Relationship

Adjustable Timing Parameters

The TM100 correction mechanism is a hybrid analog/digital implementation and has several adjustable timing parameters that allow customers to tune timing modules to the time constants of the intended applications. The adjustments also implement low pass filters to reduce crystal adjustment transients.

Supported adjustable timing parameters include:

Temperature Sample Interval – This sets the time interval (in ms) for measuring the temperature sensor and VDDA value. The interval is between 20ms and 2550ms. Both the temperature and VDDA readings are averaged over 8 sample intervals, updated at each sample interval (rolling average).

Frequency Correction Interval - This sets the time interval (in ms) for updating the Correction DAC value applied to the Varicap or external varactor. The interval is between 20ms and 2550ms.

Averaging Intervals - This sets the number of Frequency Correction Intervals used to calculate an average DAC correction value, updated each correction interval (rolling average). The averaging is between 1 and 16.

Lookup Table Curve Fit

The Lookup Table correction technique uses the measured reading from the IC temperature sensor or external thermistor (*Temp Code*) and generates a *CorrDAC Code* via a lookup table.

The lookup table is arranged from the lowest *Temp Code* to the highest *Temp Code* with up to 80 defined points. The spacing between the points is user defined to account for changing crystal temperature coefficient slopes. The appropriate DAC correction code (*CorrDac Code*) between the defined *Temp Code* points is calculated by linear interpolation.

Temp	Temp Code	CorrDAC Code
-40	2005	2720
-30	2085	2318
-20	2167	2028
-10	2250	1856
0	2333	1794
10	2416	1822
20	2500	1906
25	2542	1961
30	2584	2014
40	2669	2124
50	2754	2164
60	2841	2142
70	2923	2015
80	3009	1723
90	3096	1032

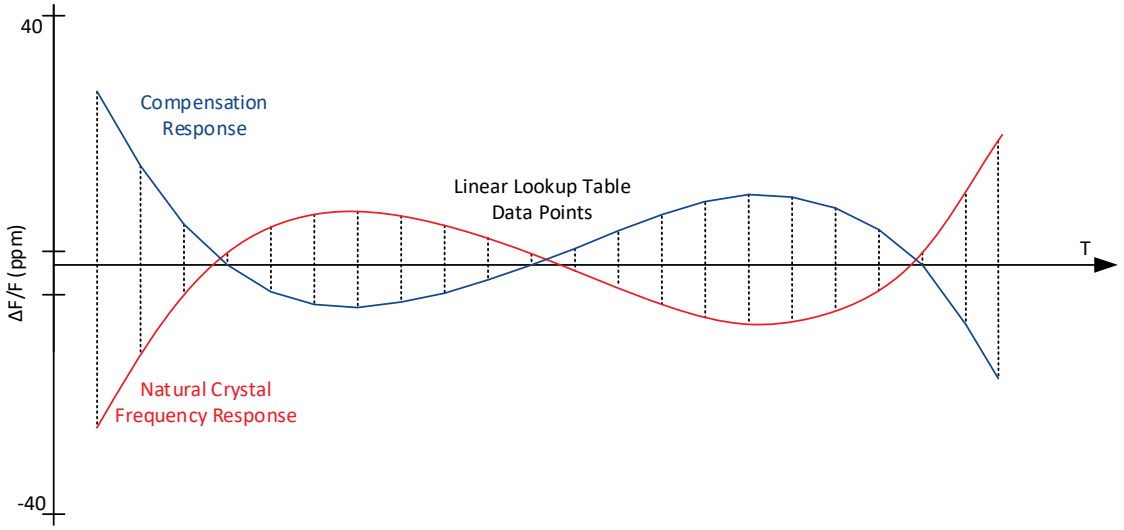


Figure 10 Linear Lookup Table Concept

Temperature Correction Polynomial Curve Fit

The temperature polynomial curve fit correction technique uses the measured temperature reading from the IC sensor or external thermistor (*Temp Code*) and calculates a *CorrDAC Voltage* via polynomial curve fit using the correction order coefficients, a_0 - a_9.

The correction process computes the Correction DAC voltage needed for best correction. The *CorrDAC Voltage* range is from 0V up the voltage of the BYPASS pin (typically, 2.9V or 3.3V depending on configuration). The correction value is converted into a 12-bit DAC input digital code (*CorrDAC Code*), 0 for 0V, and 4095 for the max BYPASS Voltage. The internal tuning Varicap operates over a range of 0V to 2.9V, so the *CorrDAC Voltage* needs to be limited when BYPASS is operated from a supply greater than 2.9V.

$$Corr_{temp}(x) = a_0 + a_1x + a_2x^2 + a_3x^3 + a_4x^4 + a_5x^5 + a_6x^6 + a_7x^7 + a_8x^8 + a_9x^9$$

$$x = TempCodeNormalized: TempCode\ normalized\ for\ Mean\ and\ Standard\ Deviation$$

$$Corr_{temp}(x) = CorrDAC\ Voltage = Correction\ DAC\ voltage$$

To use the polynomial curve fit algorithm, the following data needs to be selected or entered:

1. Desired correction order: For some applications 3rd or 5th order corrections may produce better results over temperature than a 7th or 9th order correction. This item can be set as needed for each oscillator application.

2. *Temp Code* Mean and *Temp Code* Std Dev: Measure the module over temperature and capture the *Temp Code* for each measured temperature point. Compute the mean and standard deviation of the *Temp Code* values. Then scale the *Temp Code* values by the mean and standard deviation generating *x (Temp Code Normalized)* for the above equation.

3. CorrDAC Codes over Temperature: As part of the module measurements over temperature, determine the *CorrDAC Code* that produces the least error. Convert the *CorrDAC Code* to *CorrDAC Voltage* by scaling it, 0 to 4095 for the voltage range 0 to the BYPASS pin Voltage. *CorrDAC Voltage* is $Corr_{temp}(x)$ in the equation above.

4. Use polynomial curve fit software to find the values of a_0 to a_n based on x and $Corr_{temp}(x)$.

5. Enter the coefficients, a_0 - a_9, the *Temp Code* mean, and the *Temp Code* Std Dev for the respective correction order. The coefficients are single precision floating point numbers stored in the microcontroller. Single precision floating point numbers have 7-8 decimal digits of precision and ensure that all significant digits are entered into the microcontroller.

Please refer to the separate application document titled *TMx00 Correction Algorithm Development* for details.

Supply Voltage Curve Fit

The *CorrDAC Voltage* values are not overly sensitive to supply voltage (VDDA) variation when the internal BYPASS regulator is enabled. The *Temp Code Normalized* values have some dependency on supply voltage. This means that supply voltage variations will shift the *Temp Code* values. The supply voltage polynomial curve fit correction techniques are optional enhanced correction methods that generate adjustment terms to account for this shift.

A $Corr_{voltage}$ term corrects for frequency shifts over supply voltage variation and uses the coefficients, b_1 - b_3.

A $Corr_{voltage\_temp}$ term corrects for frequency shifts from cross correlated supply voltage and temperature variation and uses the coefficients, c_1 - c_3.

The user selects whether these correction terms are applied to either the *Temp Code* or *CorrDAC Code* depending on the architecture and sensitivity of supply voltage movement of the TCXO module. Each choice has further options regarding the order of correction desired.

Temp Code Adjustment Option

Because the supply voltage range of the TMx00 is ±5%, the standard deviation of the *VDDA Code* range is set internally with respect to the nominal *VDDA Code*.

$$VDDA_{SD} = Standard\ deviation\ of\ VDDA$$

The Standard Deviation is defined so a 5% high supply voltage gives a $VDDA_{SD}$ (or σ) of +3.0, and a 5% low supply gives a $VDDA_{SD}$ of -3.0.

$$VDDA_{SD} = VDDACode_{NOM}\left(\frac{0.05}{3}\right)$$

$VDDACode_{NOM}$ is the ADC code value measured by the IC when the VDDA supply voltage is 3.3V. A typical ADC code value is 2330. Note that the VDDA ADC input is divided by 2, so the 2330 code represents an input value of 1.65V.

$$\Delta VDDA = \frac{VDDACode_{Meas} - VDDACode_{Nom}}{VDDA_{SD}}$$

Applying the correction by adjusting the *TempCode*:

$$Temp_{ADJ} = TempCodeNormalized + \Delta TempCode(\Delta VDDA)$$

Where:

$Temp_{ADJ}$ is the new *TempCodeNormalized* value input into the main $Corr_{temp}(x)$ function for frequency correction

$\Delta TempCode$ is the *Temp Code* adjustment based on voltage and temperature measurements

Temp Code $Corr_{voltage}$ 1st Order Correction Option

$$\Delta TempCode(\Delta VDDA) = Corr_{voltage}(\Delta VDDA) = b_1(\Delta VDDA)$$

Temp Code $Corr_{voltage}$ 3rd Order Correction Option

$$\Delta TempCode(\Delta VDDA) = Corr_{voltage}(\Delta VDDA) = b_1(\Delta VDDA) + b_2(\Delta VDDA)^2 + b_3(\Delta VDDA)^3$$

Temp Code $Corr_{voltage}$ & $Corr_{voltage\_temp}$ 3rd Order Correction Option

$$\begin{aligned}\Delta TempCode(\Delta VDDA) &= Corr_{voltage}(\Delta VDDA) + Corr_{voltage\_temp}(\Delta VDDA)\\ &= b_1(\Delta VDDA) + b_2(\Delta VDDA)^2 + b_3(\Delta VDDA)^3 + c_1(\Delta VDDA)(TempCode)\\ &+ c_2(\Delta VDDA)^2(TempCode) + c_3(\Delta VDDA)(TempCode)^2\end{aligned}$$

***CorrDAC Code* Adjustment Option**

Applying the correction by adjusting the *CorrDAC Code*:

$$CorrDAC_{ADJ} = CorrDAC\ Code + \Delta CorrDAC\ Code(\Delta VDDA)$$ - when using the Lookup Table Correction

Or

$$CorrDAC_{ADJ} = CorrDAC\ Voltage + \Delta CorrDAC\ Voltage(\Delta VDDA)$$ - when using the Polynomial Correction

Where:

$CorrDAC_{ADJ}$ is the new *CorrDAC Code* value output for frequency correction (Lookup Table Correction)

$\Delta CorrDAC\ Voltage$ is the new *CorrDAC Voltage* output for frequency correction (Polynomial Correction)

$\Delta CorrDAC\ Code$ is the *CorrDAC Code/Voltage* adjustment based on voltage and temperature measurements.

CorrDAC Code $Corr_{voltage}$ 1st Order Correction Option

$$\Delta CorrDAC\ Code(\Delta VDDA) = Corr_{voltage}(\Delta VDDA) = b_1(\Delta VDDA)$$

CorrDAC Code $Corr_{voltage}$ 3rd Order Correction Option

$$\Delta CorrDAC\ Code(\Delta VDDA) = Corr_{voltage}(\Delta VDDA) = b_1(\Delta VDDA) + b_2(\Delta VDDA)^2 + b_3(\Delta VDDA)^3$$

CorrDAC Code $Corr_{voltage}$ & $Corr_{voltage\_temp}$ 3rd Order Correction Option

$$\Delta CorrDAC\ Code(\Delta VDDA) = Corr_{voltage}(\Delta VDDA) + Corr_{voltage\_temp}(\Delta VDDA) = b_1(\Delta VDDA) + b_2(\Delta VDDA)^2 + b_3(\Delta VDDA)^3 + c_1(\Delta VDDA)(TempCode) + c_2(\Delta VDDA)^2(TempCode) + c_3(\Delta VDDA)(TempCode)^2$$

Correction Algorithm Implementation

Various methodologies exist for obtaining the unique crystal and TCXO module frequency responses across temperature during the manufacturing process. Please refer to the separate application document titled *TMx00 Correction Algorithm Development* for details regarding the development flow of each correction algorithm and additional information.

For more information regarding the memory structure and commands needed to program the TM100, please refer to the *TMx00 Programming Reference Manual* or use the TMx00 Control Program software to enter the values.

APPLICATION NOTES

Oscillator Power Supply Options

The BYPASS pin/net is the internal Pierce oscillator's power supply with 3 connection options. The BYPASS pin/net should be operated between 2.9V and 3.3V. (Other connections omitted)

BYPASS Shorted to VDDA

Connecting the BYPASS pin directly to the VDDA pin operates the oscillator supply voltage at 3.3V. If the incoming VDDA supply is a well-regulated low noise source, this can produce excellent oscillator phase noise performance. 22uF and 0.01uF external bypass capacitors are highly recommended located in very close proximity to the resulting supply node to reduce or eliminate spurious energy.

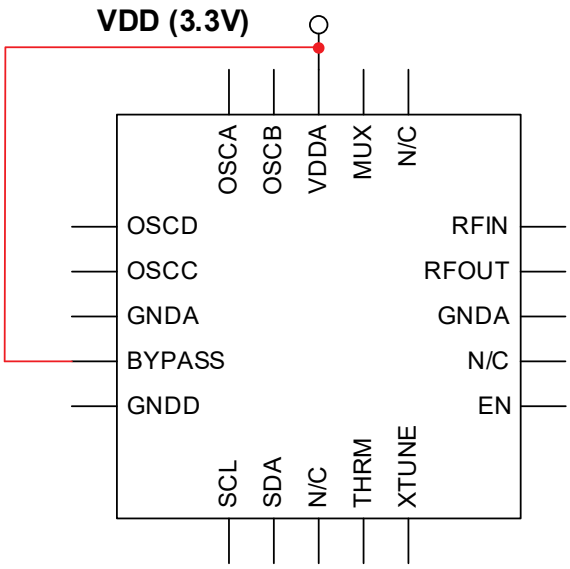


Figure 11 Oscillator Power Supply (BYPASS) Connected to VDDA

Internal BYPASS Regulator

Enabling the TM100's Internal 2.9V Regulator provides a low noise supply for the oscillator and decouples it from the VDDA supply without the need for a separate regulator. The BYPASS pin needs to have a 1nF capacitor externally to stabilize the regulator. The noise of the internal regulator is very low given the size constraints of the IC.

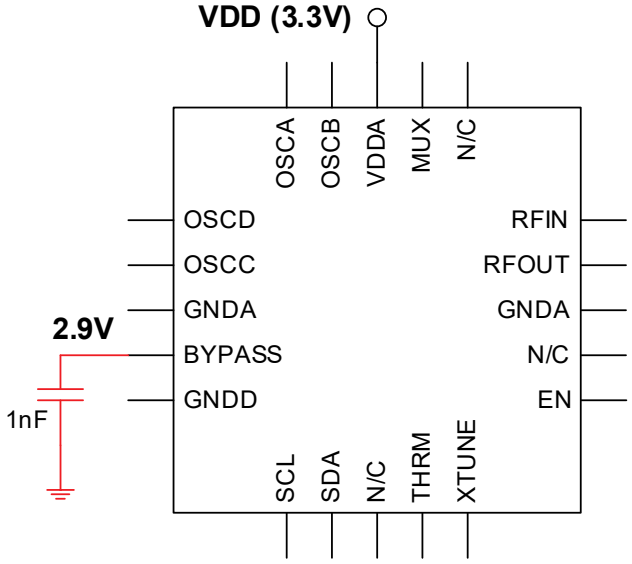


Figure 12 Oscillator Power Supply (BYPASS) Powered by Internal Regulator

External BYPASS Regulator

Connecting the BYPASS pin to an external regulator also decouples the oscillator from VDDA and can provide a lower noise supply for the oscillator for higher performance applications where the oscillator noise is below that of the internal regulator. Potential regulator choices include the Texas Instruments LP5907 or Analog Devices AD7151.

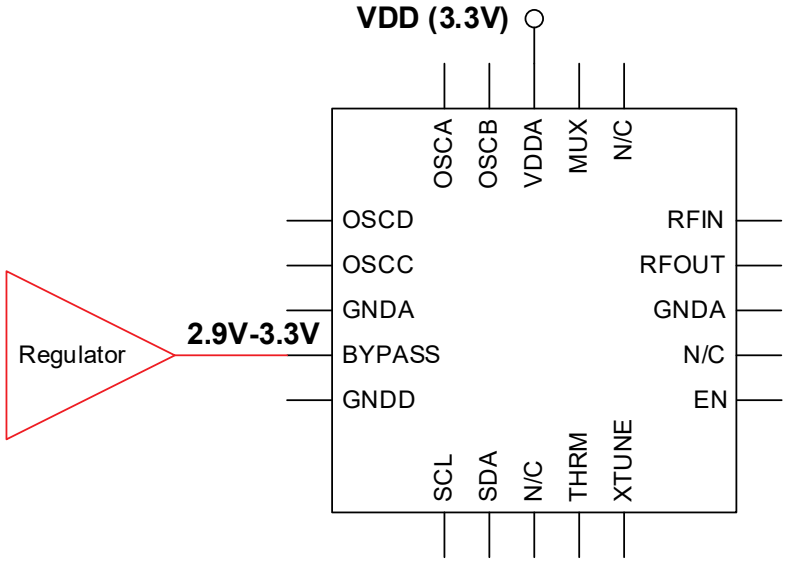


Figure 13 Oscillator Power Supply (BYPASS) Powered by External Regulator

Internal Pierce Oscillator Properties

Negative Resistance

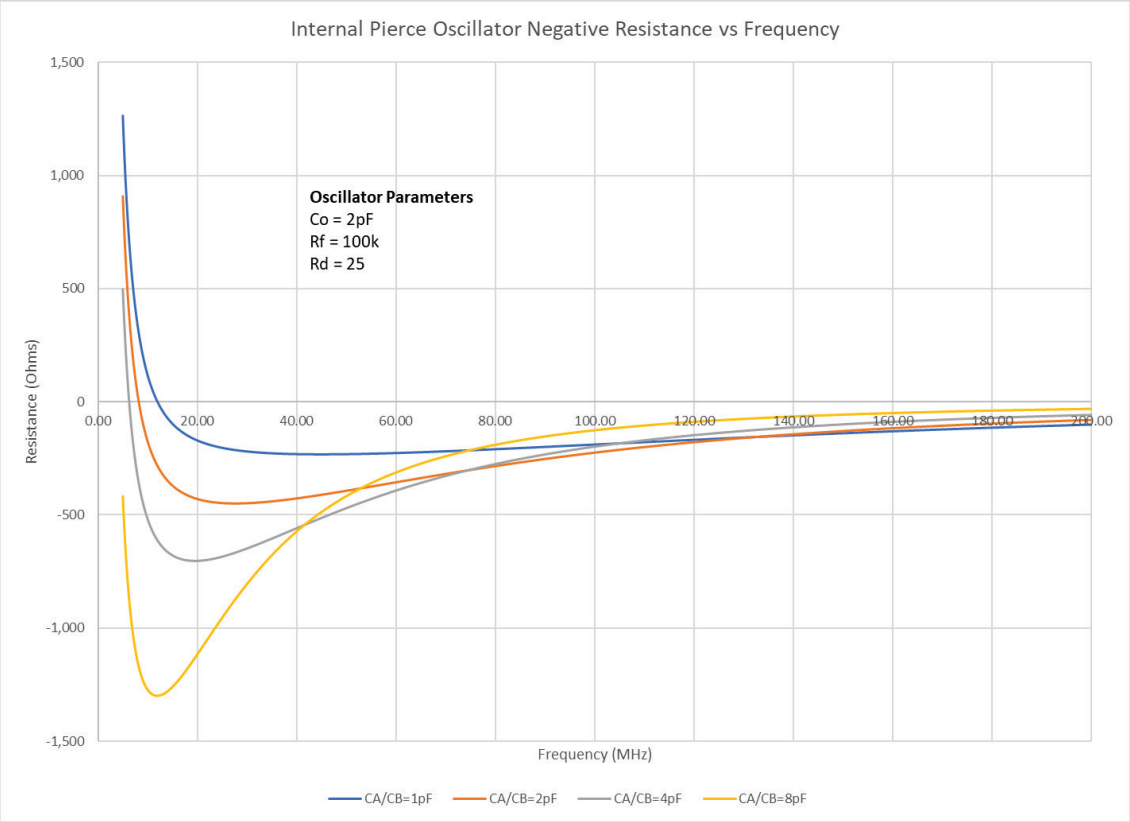


Figure 14 Pierce Oscillator Negative Resistance vs Frequency

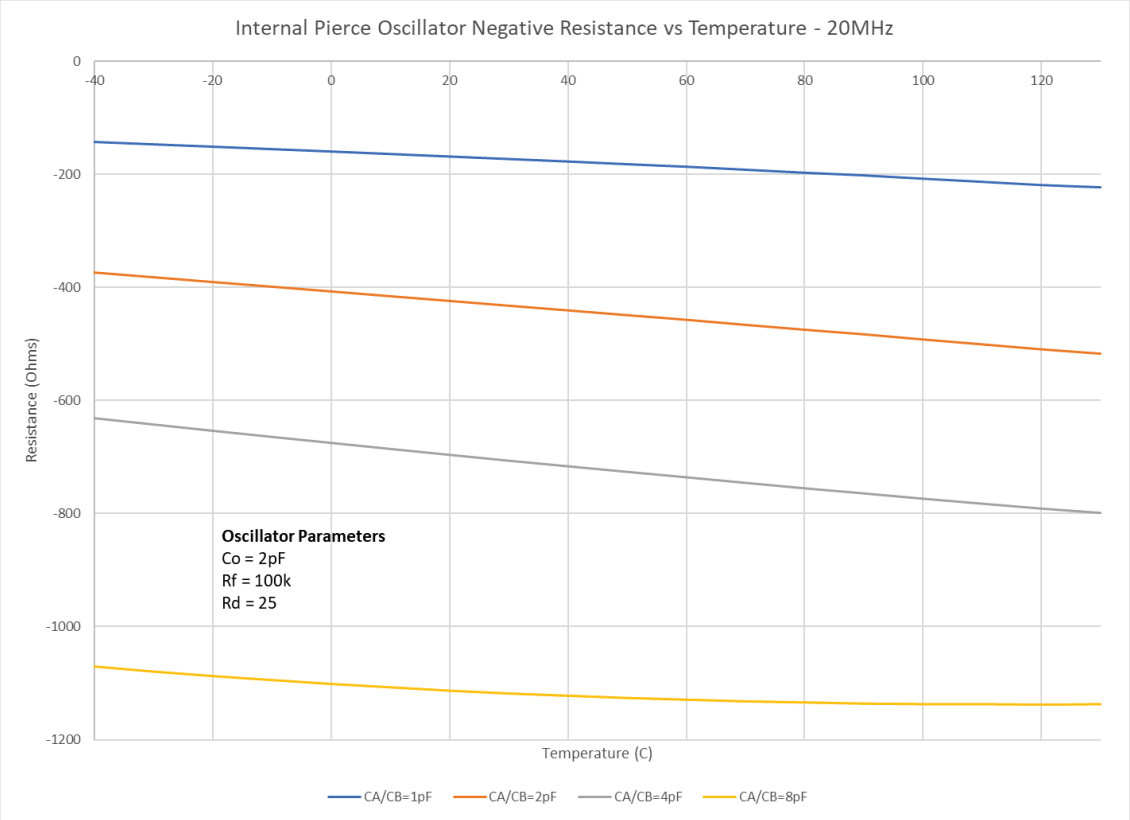


Figure 15 Pierce Oscillator Negative Resistance vs Temperature – 20MHz

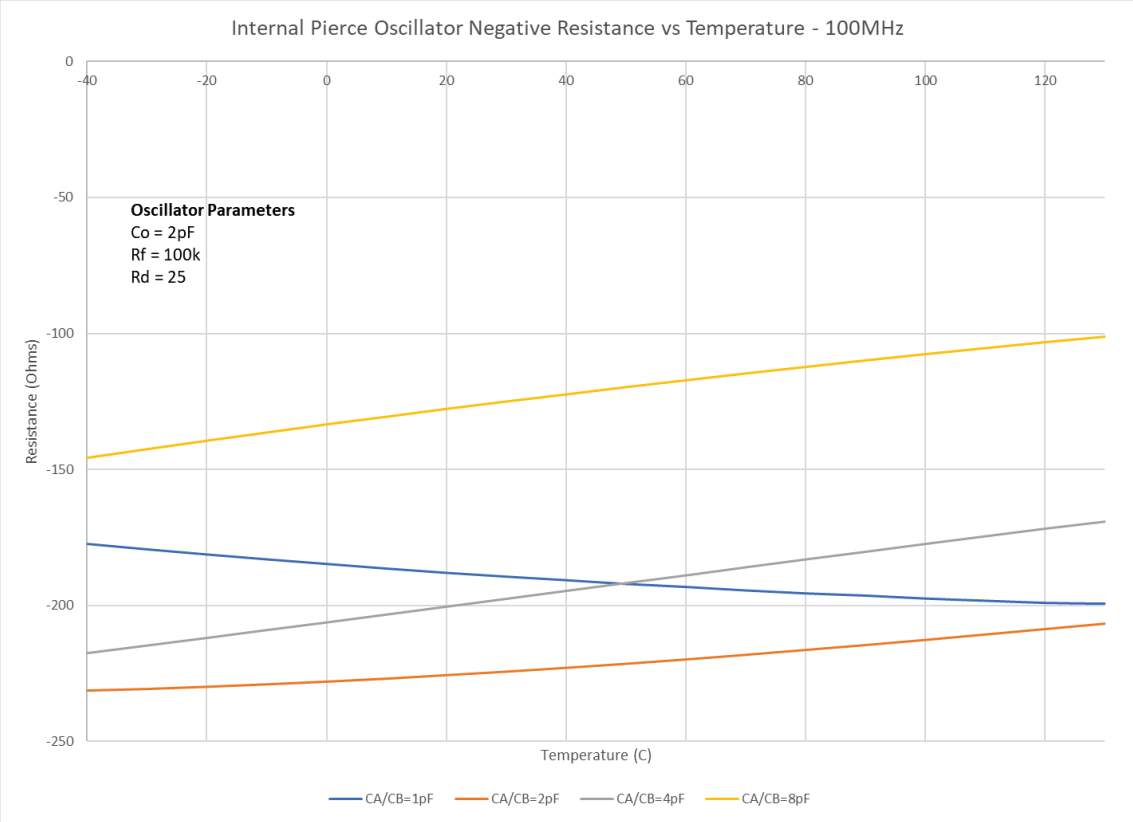


Figure 16 Pierce Oscillator Negative Resistance vs Temperature – 100MHz

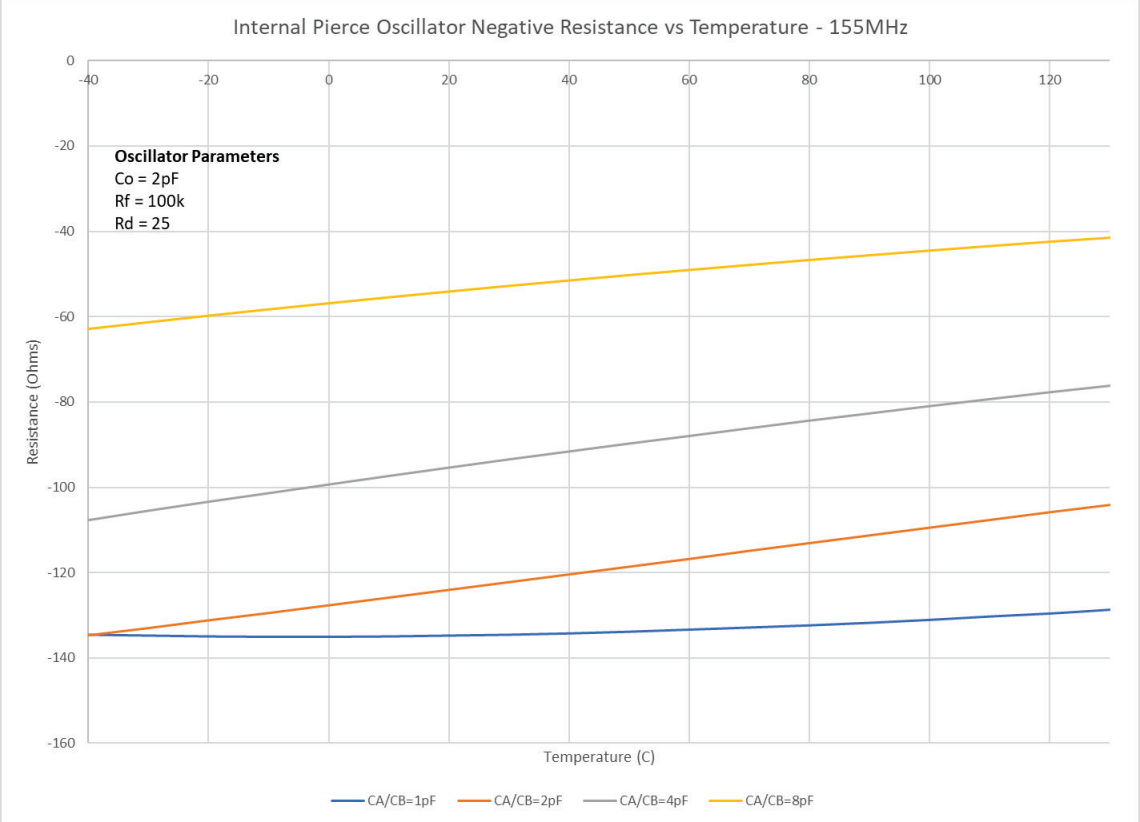


Figure 17 Pierce Oscillator Negative Resistance vs Temperature – 155MHz

Integrated Capacitors CA & CB

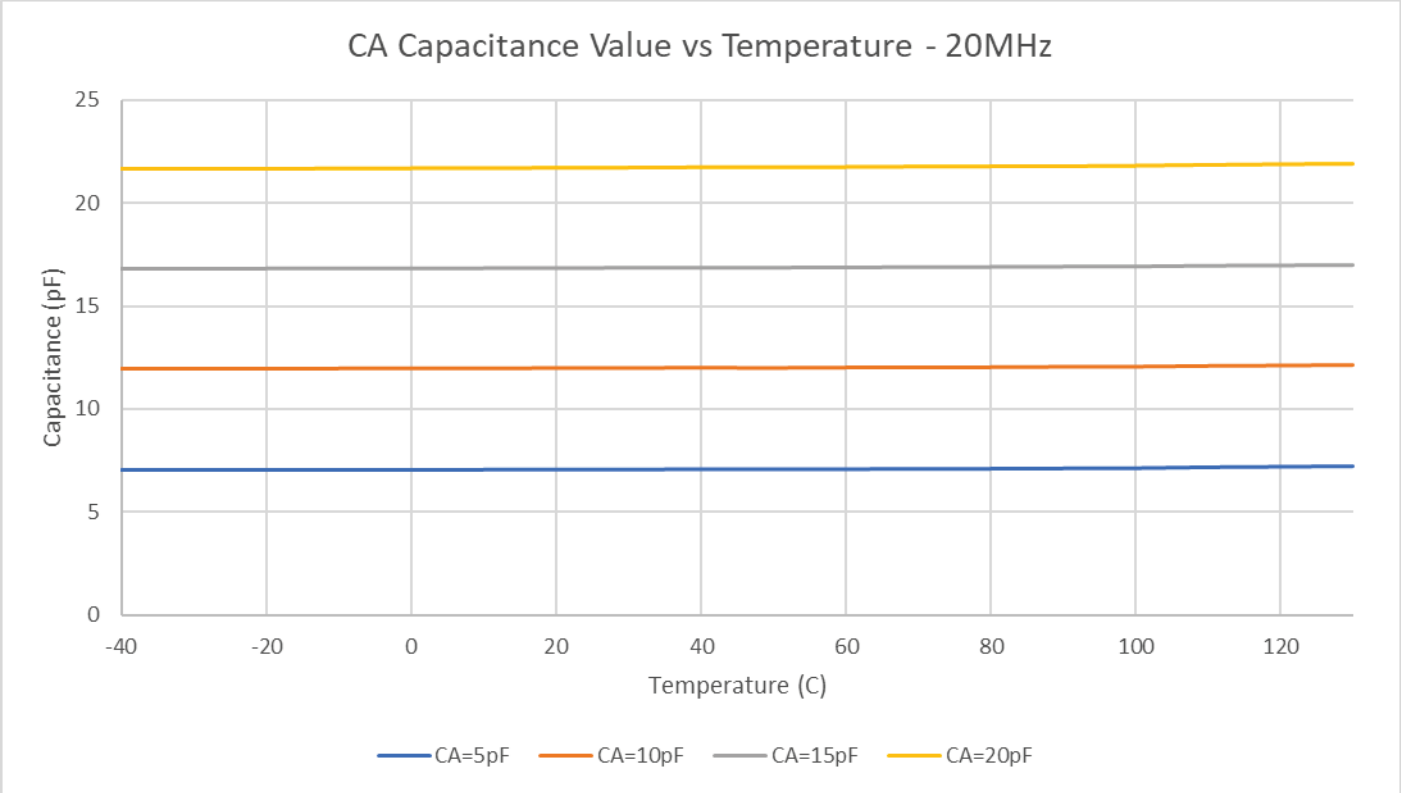


Figure 18 CA Capacitance Values vs Temperature – 20MHz

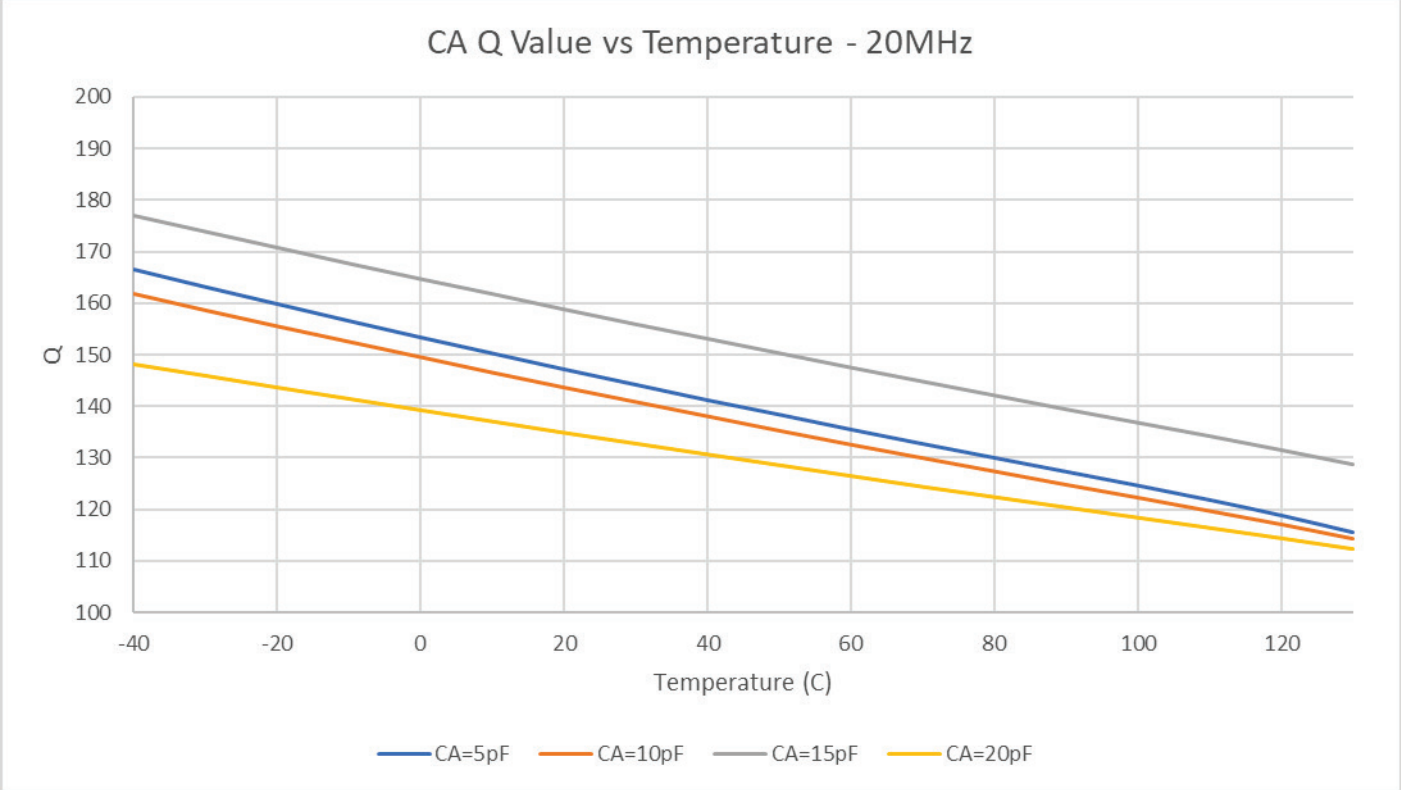


Figure 19 CA Q Values vs Temperature – 20MHz

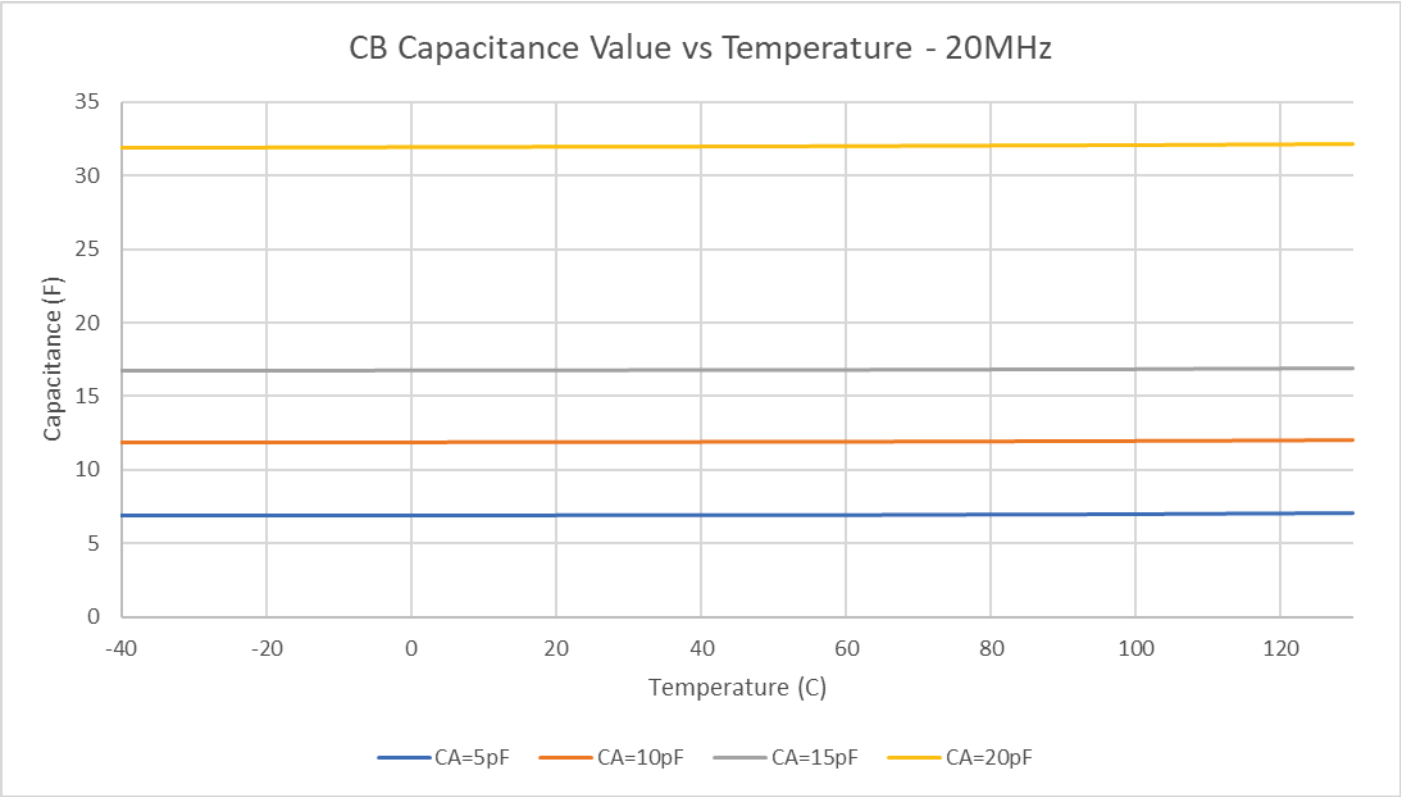


Figure 20 CB Capacitance Values vs Temperature – 20MHz

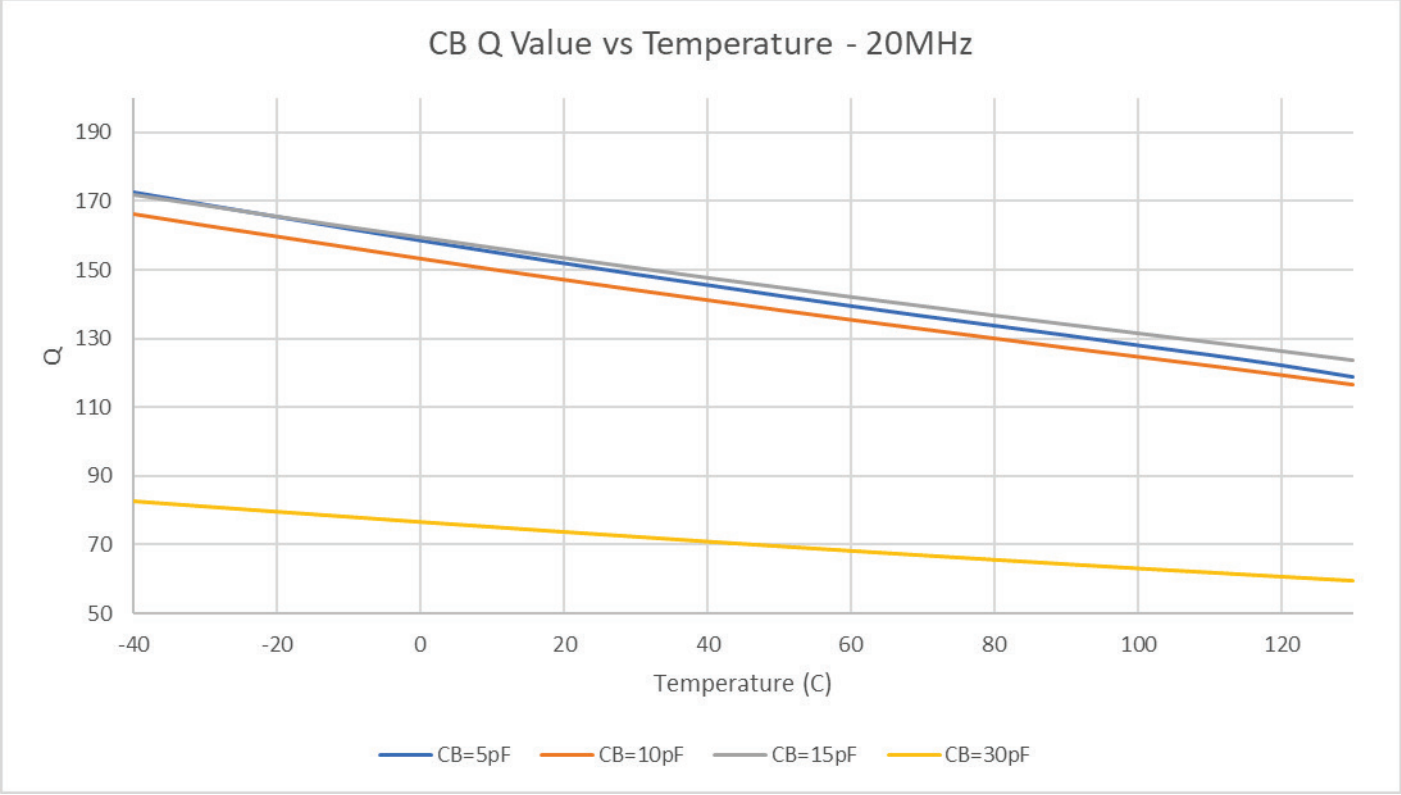


Figure 21 CB Q Values vs Temperature – 20MHz

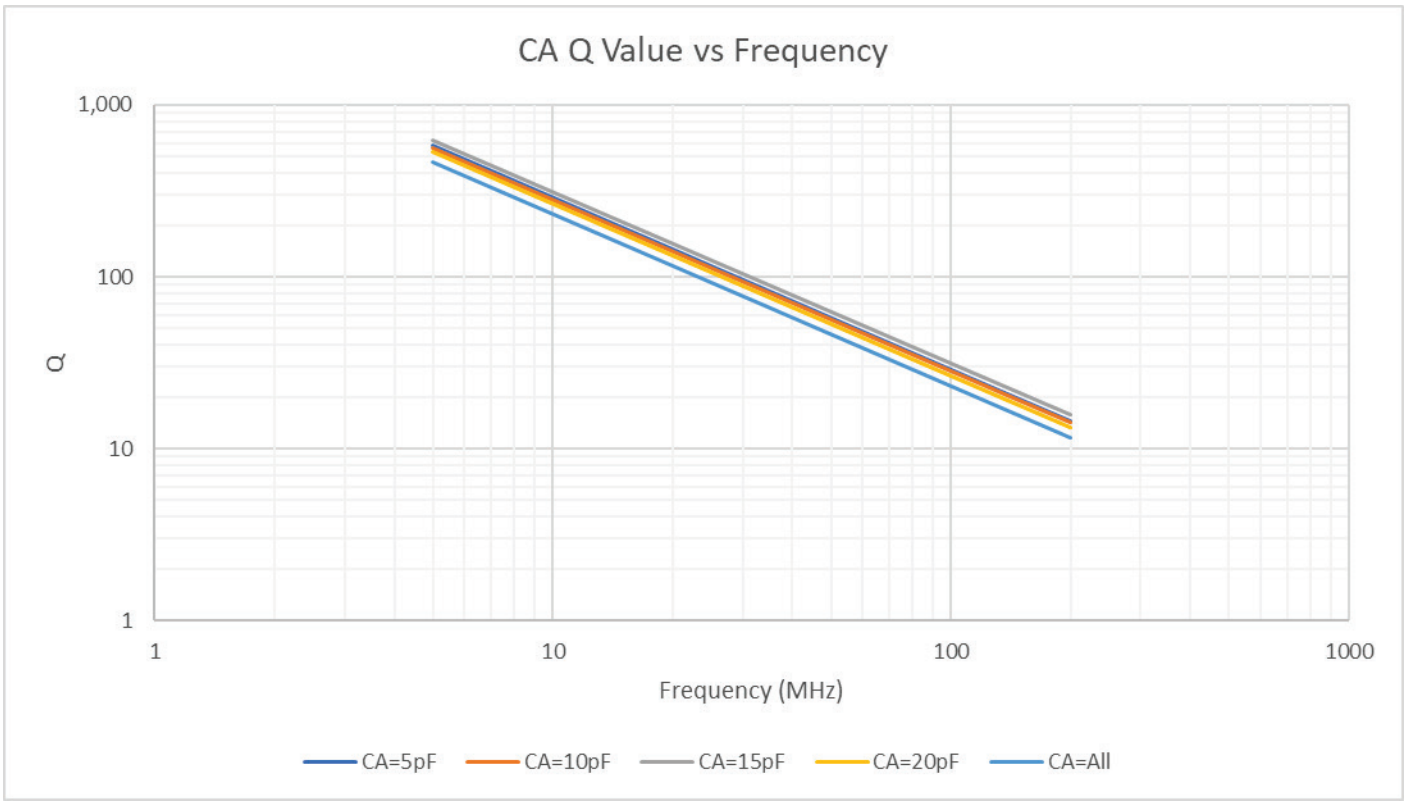


Figure 22 CA Q Values vs Frequency

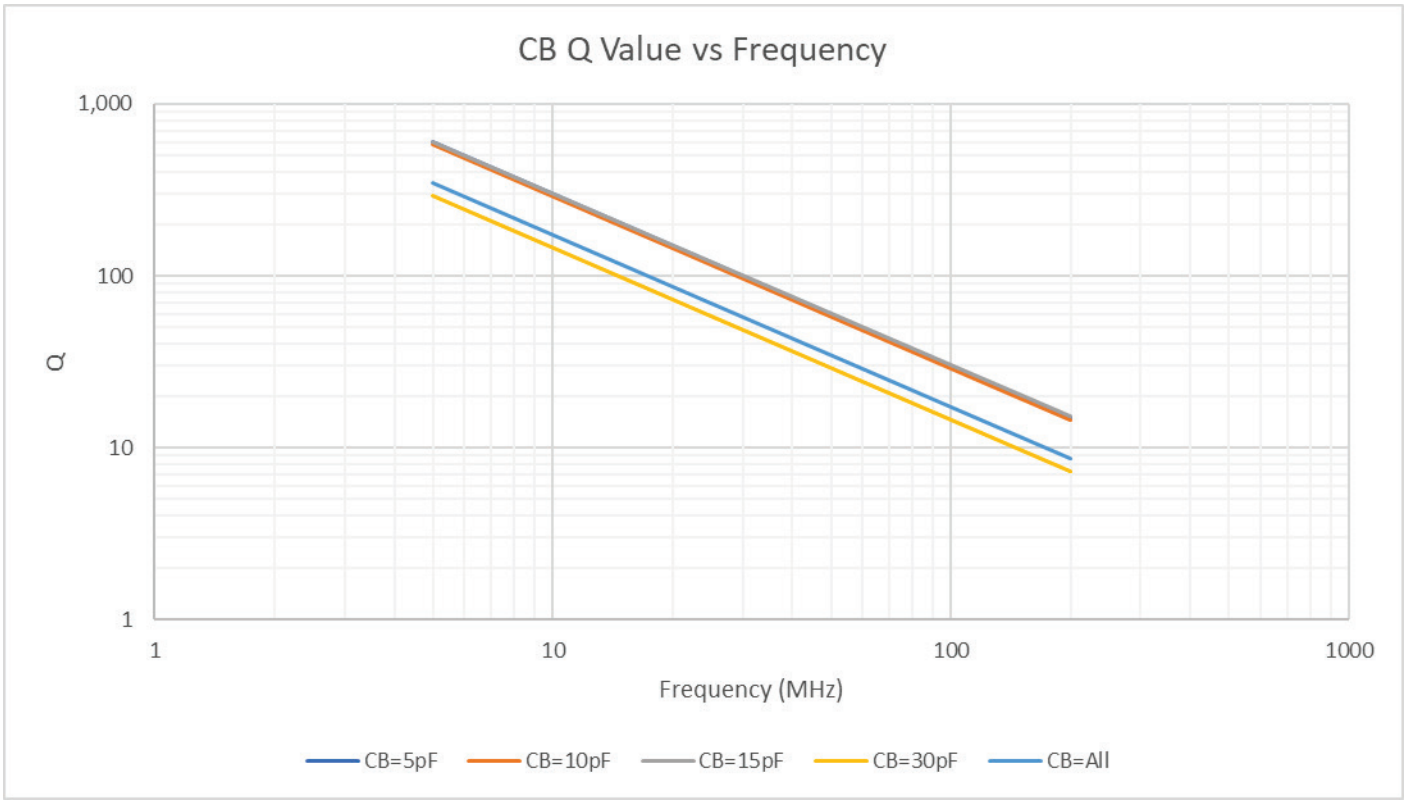


Figure 23 CB Q Values vs Frequency

Disabling Pierce Oscillator

Certain applications may require the use of an external oscillator structure. An example would be to construct a Colpitts based oscillator architecture and using the TM100 as the correction device for the oscillator. In this scenario, the internal oscillator circuit should be disabled. The proper way to disable the oscillator circuit is to do implement the following:

1. Ground the OSCA pin
2. Set C_A, C_B, C_F, C_V, and R_D to OPEN states.
3. Set R_F to 100k

Output Signal Architecture Options

The output signal can be generated with several architecture options primarily using pins RFIN and RFOUT. Other configurations are possible with careful oscillator design considerations. Output driver options include the internal TM100 RF Output Stage, an unbuffered inverter, or Hexius CF Series Fanout ICs. (Other connections omitted)

RFIN TO RF Output Stage

The internal TM100 RF Output Stage restores the clock edges, makes duty cycle adjustments, and performs any necessary clock division before driving the output load. The RF Output Stage is an effective alternative to using external ICs to condition the output signal of an TCXO module. With this configuration, the MCU may be clocked with the internal ring oscillator or switched over to the crystal oscillator.

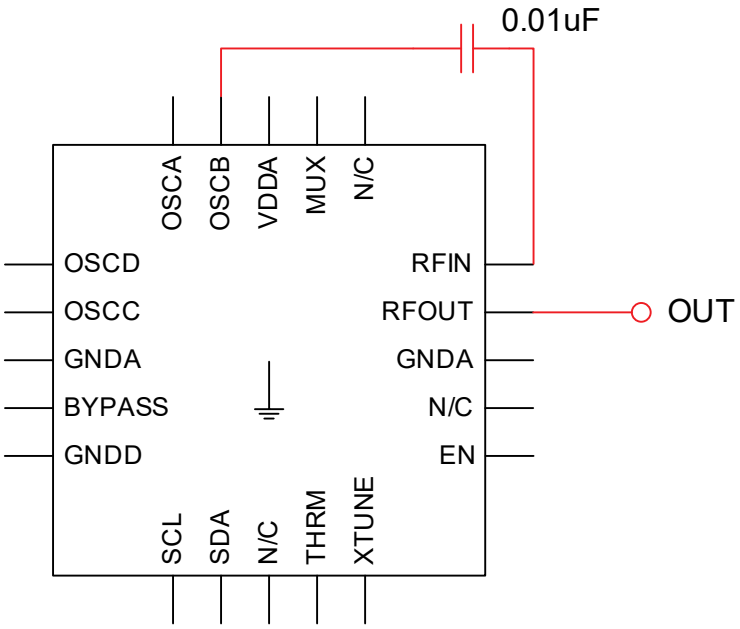


Figure 24 RFIN to RF Output Stage Option

RFIN into Inverter

If the RF Output Stage features are not needed, driving the unbuffered inverter from RFIN produces excellent phase noise floor performance while retaining the ability for duty cycle adjustment and MCU clock control. With this configuration, the MCU may be clocked with the internal ring oscillator or switched over to the crystal oscillator. The RFOUT stage needs to be disabled and the RFOUT pin should be left unconnected.

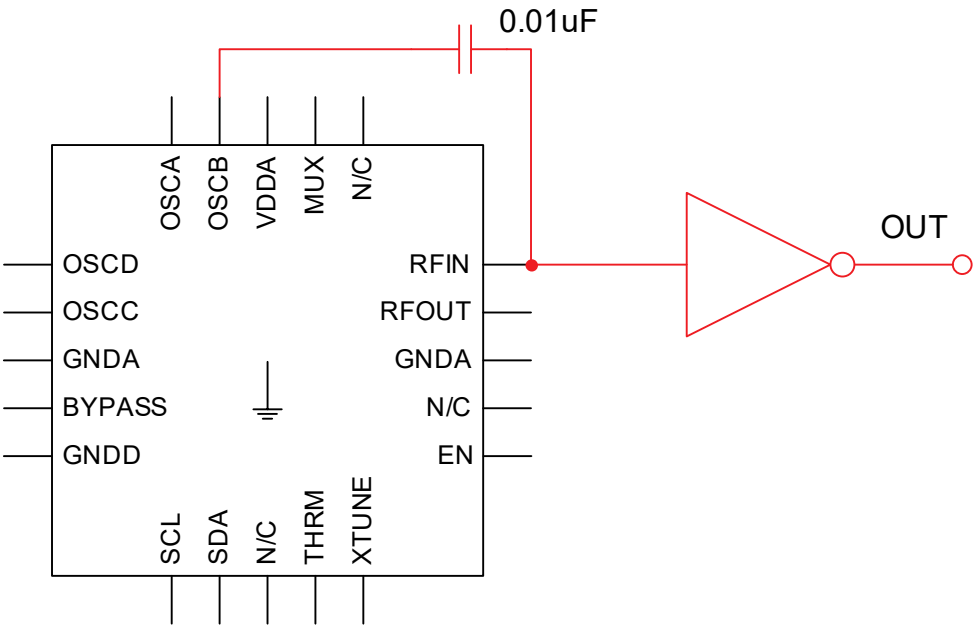


Figure 25 RFIN to Unbuffered Inverter Option

RFIN into Hexius CF Series Fanout Buffer

Another option that produces multiple output signals is to use Hexius' CF Series of fanout buffer that produce CMOS or LVPECL outputs. The CF Series fanout buffers have frequency division and industry leading extremely low additive jitter. With this configuration, the MCU may be clocked with the internal ring oscillator or switched over to the crystal oscillator. The RFOUT stage needs to be disabled and the RFOUT pin should be left unconnected.

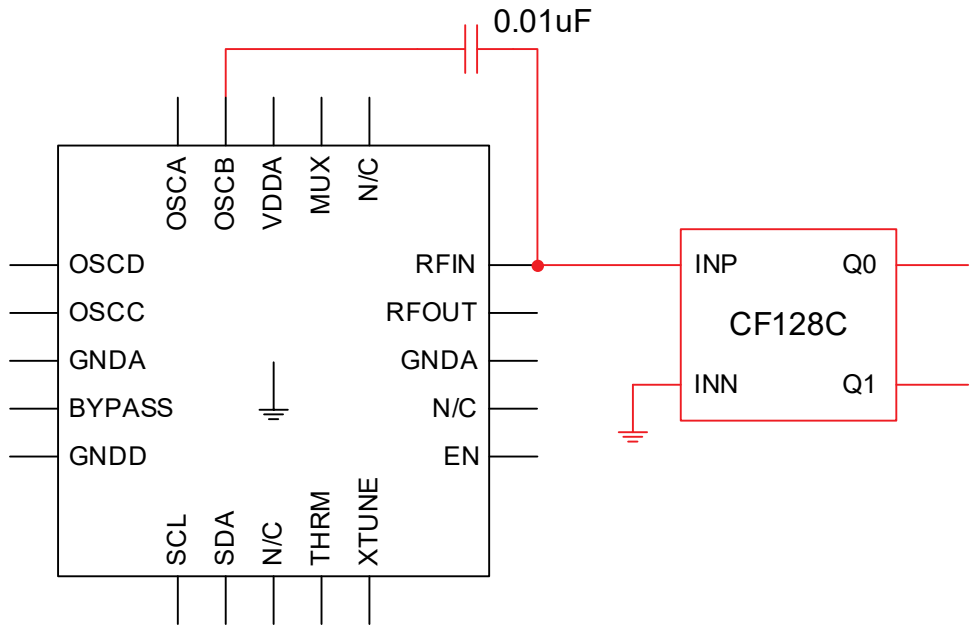


Figure 26 RFIN to Hexius CF Series Fanout Buffer

MCU Clock Source Selection

As mentioned in the Microcontroller Clock Source description, the MCU can be clocked using the internal ring oscillator within the TM100 or by the crystal oscillator itself. Upon startup, the MCU must be initially clocked by the internal ring oscillator because the crystal oscillator is not yet available. *However, the ring oscillator is noisy and asynchronous compared to the crystal oscillator, so it is advantageous to run the MCU from the crystal oscillator for better phase noise floor performance and less spurious energy.*

The TM100 is designed to have the MCU clock source switch over glitch-free from the ring oscillator to the crystal oscillator once it detects stable oscillator operation. This operation must be selected by the user otherwise the TM100 will continuously run off the ring oscillator. Please refer to the *TMx00 Control Software & EVB Kit Guide* for instructions on how to do this using the TMx00 Control Software and the *TMx00 Programming Reference Manual* for how to do this via I2C commands.

The MCU target clock speed is between 1 and 10 MHz, so internal frequency dividers can provide the proper clock rate for TCXO outputs exceeding 10MHz. If the crystal oscillator signal fails, the TM100 will automatically switch back to the ring oscillator so that MCU functionality and communication can be maintained.

External Thermistor (THRM Pin)

The THRM pin is an external thermistor input that replaces the internal temperature sensor to support direct monitoring of the crystal temperature. A typical circuit is shown in Figure 27. The thermistor has a negative temperature coefficient so the voltage on the THRM pin increases as the temperature increases. The voltage on the pin is scaled by the parallel resistor R0 and the series resistor R1.

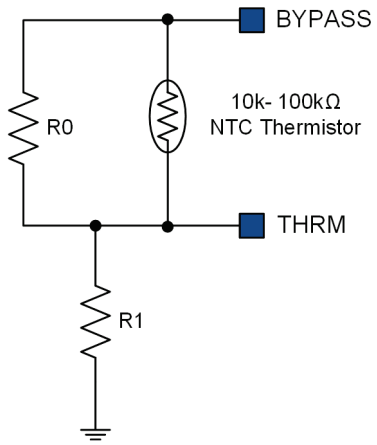


Figure 27 Typical External Thermistor Circuit

The resistance of Negative Temperature Coefficient thermistors is defined as:

$$R_T = R_0 * e^{\beta*(\frac{1}{T}-\frac{1}{T_0})}$$

Typical values for the thermistor R_0 are 10k, 20k, 50k, or 100k at 25 C. Beta values depend upon the manufacturer and type, with typical values of 3500 to 4500.

External Thermistor Implementation Example

Design Variables:

BYPASS = 2.9 Volts

Maximum Operating (correction) Temperature: 90 C

Minimum Operating (correction)Temperature: -40 C

Thermistor: R_0@25 C = 100k

Beta = 3.97k

Set R0 and R1 so that the maximum voltage at 90 C is 2.6 V. R1 is the primary determinant of this voltage. This configuration allows good temperature step resolution at the high end and sufficient headroom for thermistor operation. Next set R0 and R1 (mostly R0) so the minimum voltage is a few tenths of a volt. In this case the minimum voltage is 0.3V. The values selected are 806KΩ for R0 and 80.6KΩ for R1.

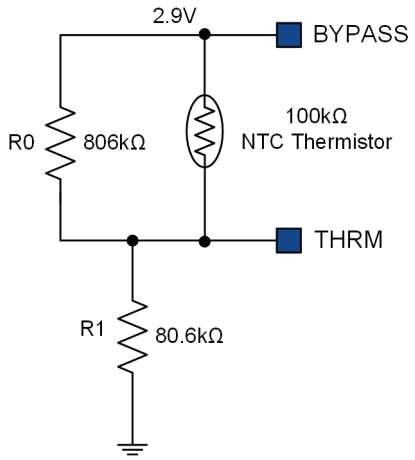


Figure 28 Thermistor Circuit Example

Figure 29 shows the resultant voltage curve over the operating temperature range. Note that the voltage is not a linear function of temperature. The firmware in the MCU properly handles the curvature so the proper DAC code can be sent to the Internal Varicap or external varactor for frequency tuning. Since the correction temperature range is reduced, the effective correction temperature step is also reduced.

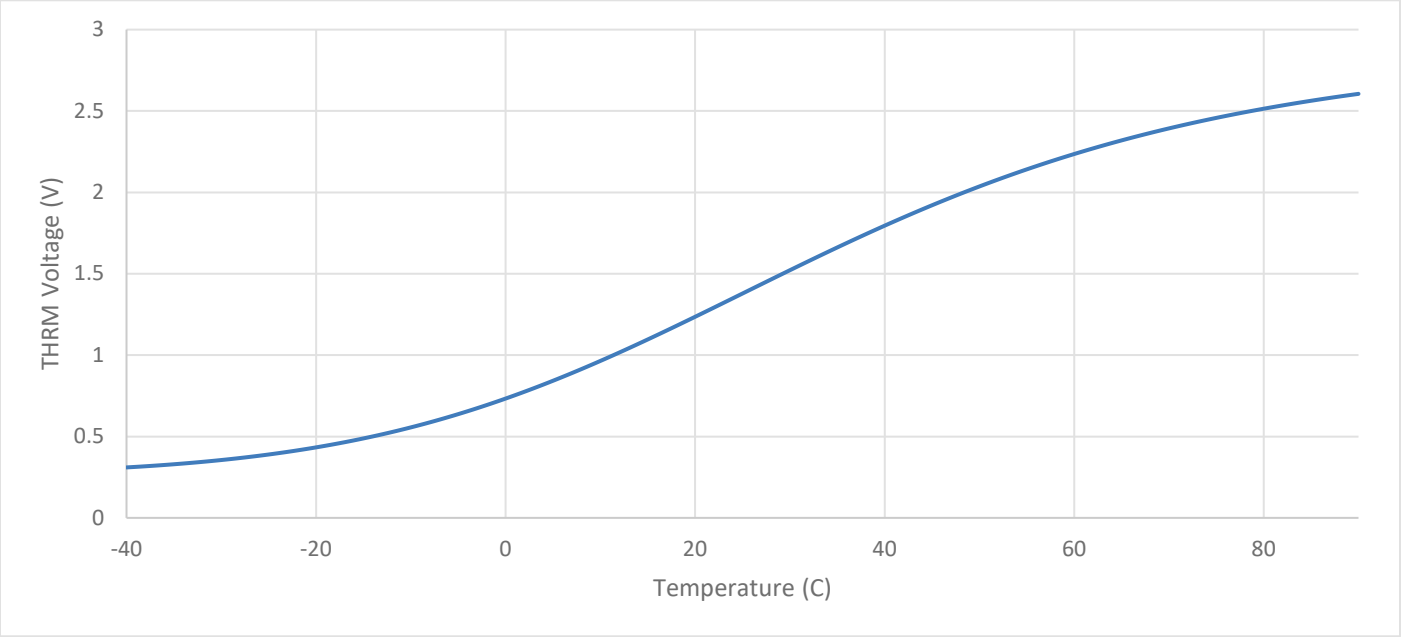


Figure 29 External Thermistor Circuit Transfer Curve

DESIGN EXAMPLE

The design example described below is one of many different possibilities as the TM100 supports many different types of oscillator architectures and TCXO module construction configurations. The example below is used to present one such configuration and its performance. This example uses a 20MHz fundamental AT-Cut crystal with the internal Varicap of the TM100, an unbuffered CMOS inverter output driver, and external thermistor for crystal temperature sensing.

Oscillator

The oscillator uses a 20MHz fundamental AT-Cut crystal with the internal Varicap and an unbuffered CMOS inverter output driver. This configuration can produce better phase noise floor performance by bypassing the additional stages in the RF Output Stage that provide increased functionality. Alternatively, output signal fanout and frequency division functionality with extremely low additive jitter can be achieved with the Hexius CF Series Fanout Buffers.

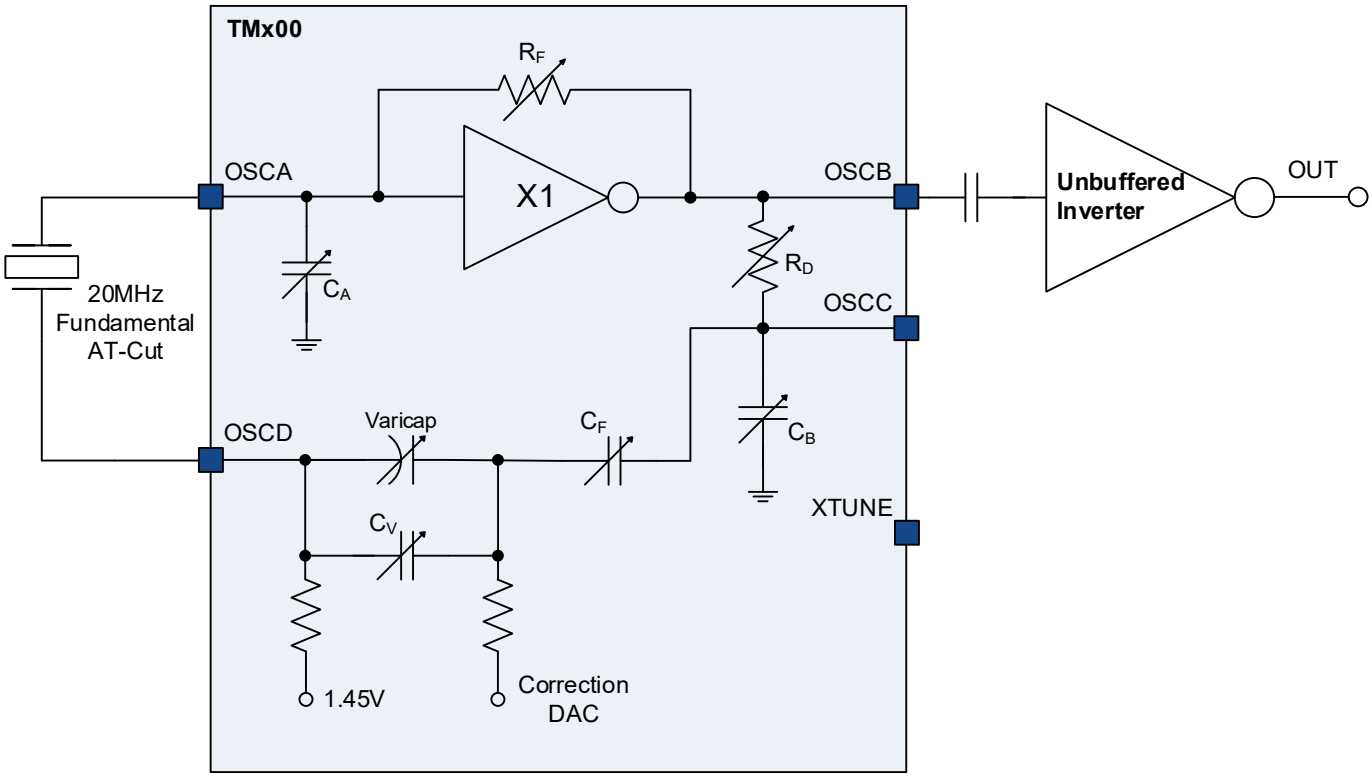


Figure 30 Oscillator Design Example

TCXO Module

A TCXO module can be constructed using the above oscillator design in the schematic shown below. The configuration uses an external thermistor network to monitor the crystal temperature (alternatively, the TM100's internal temperature can be used). The oscillator supply (BYPASS) connects directly to VDD and an unbuffered inverter provides the best phase noise floor for the output signal. Note the bypass caps that should be used externally of the module.

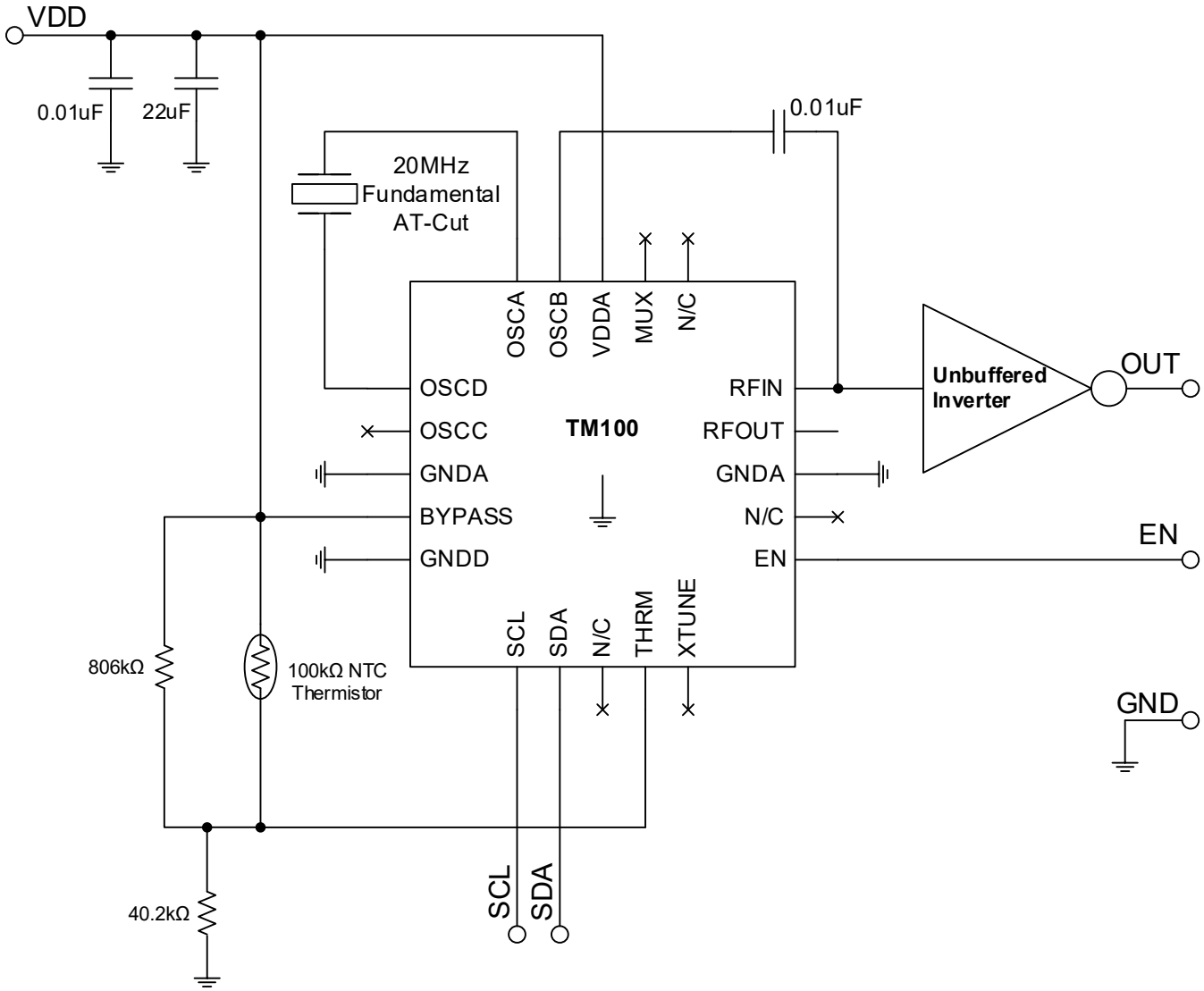


Figure 31 TCXO Module Design Example

Phase Noise Performance

The oscillator configuration described above in conjunction with a 5032 20MHz crystal produces the following phase noise plot and is typical of many crystals. Many variables external to the TM100 contribute towards the phase noise performance of any oscillator and requires thoughtful design to meet an application's specifications. Most of the spurs seen in plot below are artifacts of the Holzworth Phase Noise Analyzer and the evaluation board. This design example achieves an integrated jitter performance of 31fs and with a phase noise floor of roughly -175dBc/Hz. Updated and refined phase noise performance will be presented in future revisions of the datasheet and within the *TMx00 Design Example Manual*.

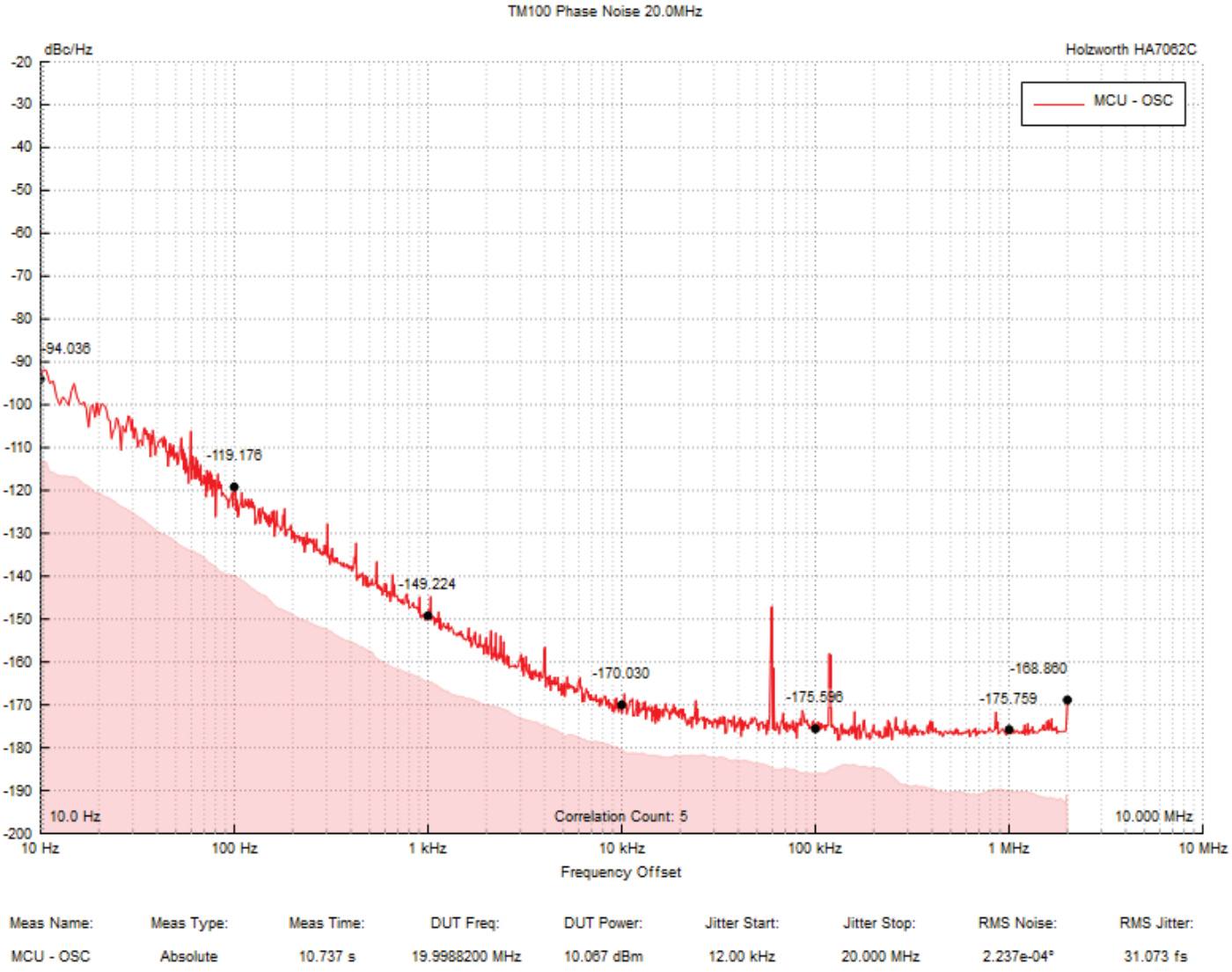


Figure 32 Phase Noise Performance

Crystal Characterization

The crystal characterization methodology of this design example is described in the *TMx00 Correction Algorithm Development for Characterization & Manufacturing* document. Using this methodology, the temperature (TempCode) and crystal correction voltage (CorrDAC Code) relationship is determined. The TM100 uses this data to implement a Linear Lookup Table or Polynomial correction.

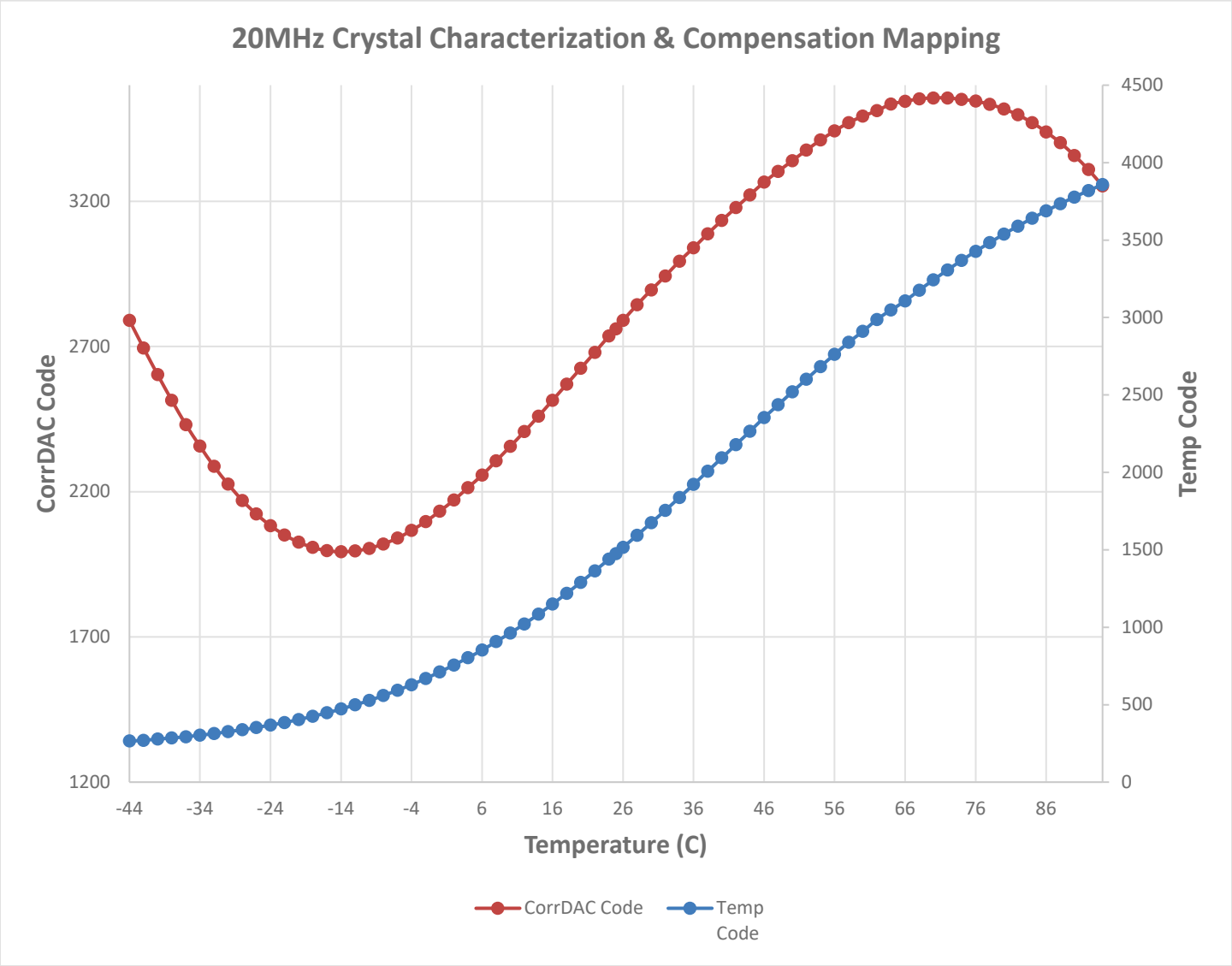


Figure 33 Crystal Characterization & Compensation Curves

Frequency Stability

The TM100 has the ability to compensate for frequency variations across temperatures below 25ppb with proper TCXO module construction, frequency-temperature characterization, and correction algorithm implementation. The IC provides the control and computational power to achieve very tight frequency stability performance, but the performance ultimately depends on the user's ability to achieve tight thermal coupling and detailed characterization of a TCXO module design. This design example uses a Linear Lookup Table correction algorithm to achieve a ±25ppb frequency stability across a temperature range of -44C to 94C.

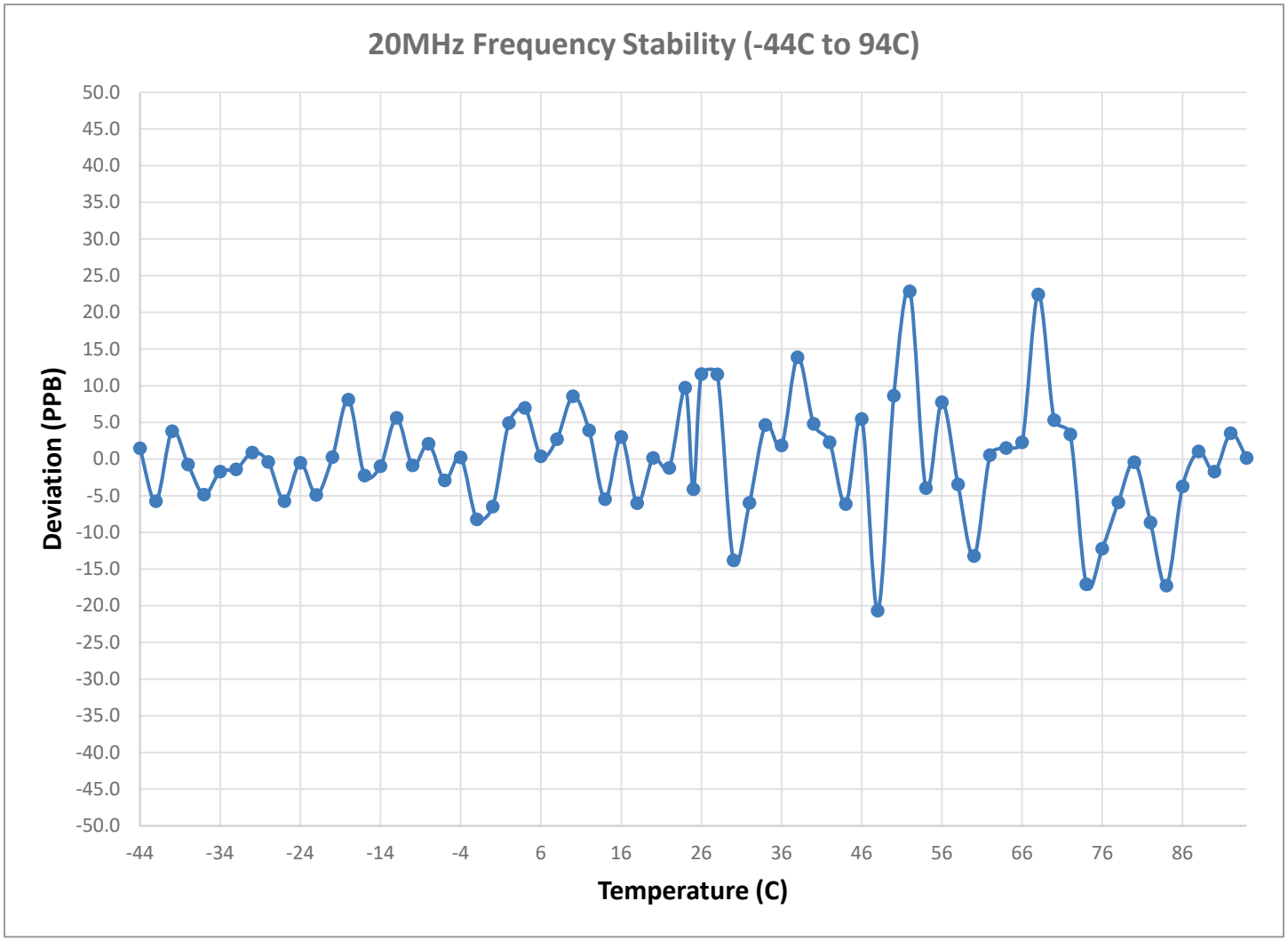


Figure 34 Frequency Stability Performance

Other Design Examples

Many other design examples are feasible with the TM100 to include 3OT crystals and various frequency ranges. Please refer to the *TMx00 Design Example Manual* for additional examples of various oscillator architectures that can be built with the TM100. The Hexius EB-TMx00 Evaluation board supports many of the possible options for rapid prototyping. Please contact Hexius Semiconductor for support in developing oscillator configurations and TCXO modules for your specific application.

PCB CONSIDERATIONS

Power Supply Filtering

On-chip regulation, power supply filtering and good PCB layout all contribute to minimizing power supply noise. For optimal performance the TM100 should be isolated from the power supply noise with the following guidelines:

1. Power supply traces need to be appropriately sized for the current demands.
2. Place a 22uF bypass capacitor from the power supply to the device's supply pins. An 0805 or larger X7R ceramic or tantalum capacitor is recommended.
3. One set of bypass capacitors values of 22uF, 0.1uF & 0.01uF should be placed as close as possible to the device.

Signal Traces

Improper routing of the signals of the TM100 can have adverse effects on the performance and therefore must be treated with care. Signals should not be treated as digital signals but rather high-performance RF analog signals otherwise system performance may be degraded. Signal routing guidelines include:

1. Physically locate the signal source as close to the load as possible
2. Limit the length of traces
3. Do not run signals through or near large FPGAs (or similar) with lots of switching activity and various frequencies
4. Do not run signals adjacent to digital data lines
5. Avoid routing signals near or alongside digital lines
6. Avoid crossing digital traces on an adjacent PCB planes
7. Shield signals with ground planes, adjacent traces, or both
8. Try to keep clock trace routes straight; if turns are necessary, make them with round bends

DIE & PAD COORDINATES

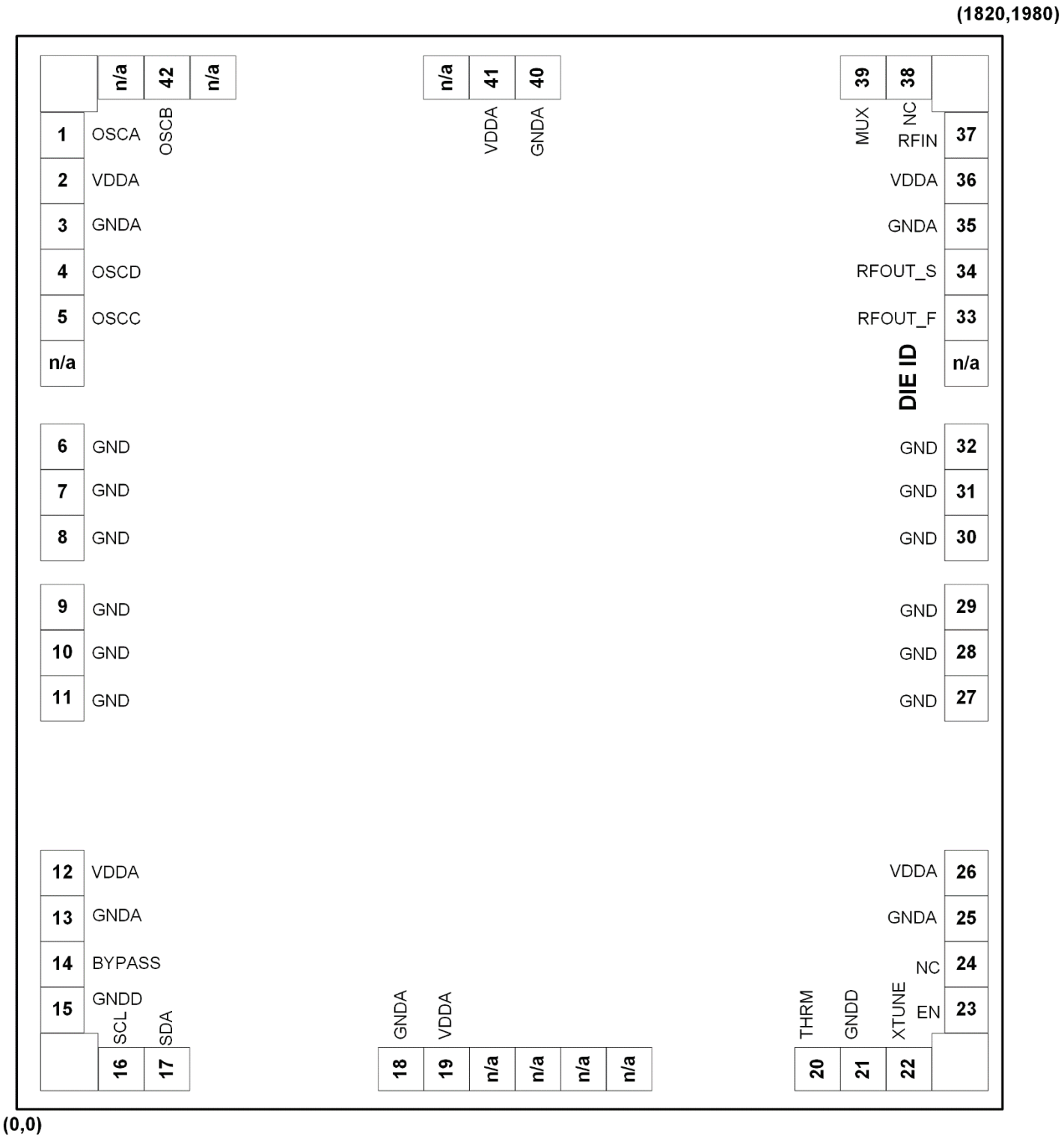


Figure 35 Die Pad Locations

Table 10 Pad Coordinates

Pad	Pad Name	I/O/P	Description	X (um)	Y (um)	Bonded in Package
1	OSCA	I/O	Pierce Inverter Stage Input From Crystal	74.20	1797.04	Yes
2	VDDA	P	3.3V Analog Positive Supply	74.20	1712.80	No
3	GNDA	P	Analog Ground	74.20	1628.56	No
4	OSCD	I/O	Crystal drive	74.20	1544.32	Yes
5	OSCC	I/O	Crystal drive	74.20	1460.08	Yes
6	GND	P	Ground	74.20	1222.32	Yes
7	GND	P	Ground	74.20	1138.08	Yes
8	NC/GND	P	Not Connected / Ground	74.20	1053.84	Yes
9	NC/GND	P	Not Connected / Ground	74.20	926.40	Yes
10	GND	P	Ground	74.20	842.16	Yes
11	GND	P	Ground	74.20	757.92	Yes
12	VDDA	P	3.3V Analog Positive Supply	74.20	435.92	No
13	GNDA	P	Analog Ground	74.20	351.68	No
14	BYPASS	I/O	Osc Regulator Voltage (2.9V)	74.20	267.44	Yes
15	GNDD	P	Digital Ground	74.20	183.20	Yes
16	SCL	I/O	I^2C Clock	183.20	74.20	Yes
17	SDA	I/O	I^2C Data	267.44	74.20	Yes
18	GNDA	P	Analog Ground	699.52	74.20	No
19	VDDA	P	3.3V Analog Positive Supply	783.76	74.20	No
20	THRM	I	Thermistor Input	1468.56	74.20	Yes
21	GNDD	P	Digital Ground	1552.79	74.20	No
22	XTUNE	O	Adjustable Tuning Voltage	1637.04	74.20	Yes
23	EN	I/O	Enable	1743.26	183.20	Yes
24	N/C	n/a	Not Connected	1743.26	267.44	No
25	GNDA	P	Analog Ground	1743.26	351.68	No
26	VDDA	P	3.3V Analog Positive Supply	1743.26	435.92	No
27	GND	P	Ground	1743.26	757.92	Yes
28	GND	P	Ground	1743.26	842.16	Yes
29	NC/GND	P	Not Connected / Ground	1743.26	926.40	Yes
30	NC/GND	P	Not Connected / Ground	1743.26	1053.84	Yes
31	GND	P	Ground	1743.26	1138.08	Yes
32	GND	P	Ground	1743.26	1222.32	Yes
33	RFOUT_F	O	Fast RF Output - 3.3V	1743.26	1460.10	Yes
34	RFOUT_S	O	Slow RF Output - 3.3V	1743.26	1544.32	Yes
35	GNDA	P	Analog Ground	1743.26	1628.56	No
36	VDDA	P	3.3V Analog Positive Supply	1743.26	1712.80	No
37	RFIN	I/O	Oscillator Input to Output Stage	1743.26	1797.04	Yes
38	N/C	n/a	Not Connected	1637.04	1903.26	No
39	MUX	I/O	General Purpose MUX Input	1552.80	1903.26	Yes
40	GNDA	P	Analog Ground	952.24	1903.26	Yes
41	VDDA	P	3.3V Analog Positive Supply	868.00	1903.26	Yes
42	OSCB	I/O	Pierce Inverter Stage Output	267.44	1903.26	Yes

DIE BONDING GUIDANCE

Bonding the TM100 die into a module will depend heavily on the circuit architecture that it is configured for. As a result, it is difficult to recommend a definitive bonding diagram for a die application. The packaged version of the TM100 is designed for maximum configurations but may not represent the optimum bonding for a specific module using the TM100. As a starting reference, Table 11 states which pads are bonded in the packaged version of the TM100.

Oscillator Pad Connections – Pads 1, 4, 5, 42

If the oscillator circuit of the TM100 is being used, OSCA (1) and OSCB (42) will need to be bonded. Bonding OSCC (5) and/or OSCD (4) will depend on the oscillator configuration and what TM100 internal devices are used. For example, if the internal Varicap of the TM100 is being used for the oscillator circuit, OSCD needs to be bonded.

Analog Power Supply (VDDA) – Pads 2, 12, 19, 26, 36, 41

The TM100 has multiple analog supply pads throughout the pad ring for robust ESD protection. Only one of these power supply pads need to be connected to power the 3.3V analog rail. The packaged version of the TM100 uses pad 41. Multiple pads may be connected.

Analog Ground Supply (GNDA) – Pads 3, 13, 18, 25, 35, 40

The TM100 has multiple analog ground pads throughout the pad ring for robust ESD protection. Only one of these power supply pads need to be connected to power the 0V analog rail. The packaged version of the TM100 uses pad 40. Multiple pads may be connected.

GND Pad Connections – Pads 6, 7, 10, 11 & Pads 27, 28, 31, 32

These pads support a function not used for TM100 functionality but should be connected to ground. There are two sets of these pads but only one from each set needs to be grounded. Pads 6, 7, 10, 11 are one set and pads 27, 28, 31, 32 are the other set. For example, connecting pad 6 and pad 32 to ground satisfies the connection requirements. GND may be shorted to GNDA outside of the IC.

Digital Ground Supply (GNDD) – Pads 15, 21

Separating the digital ground from the analog ground is essential in reducing spurious energy so a separate ground exists that needs to be bonded. The packaged version only bonds pad 15 but bonding both pad 15 and 21 is a good idea. GNDD may be shorted to GNDA outside of the IC.

Communication Connections (SCL, SDA, EN) – Pads 16, 17, 23

SCL and SDA must be bonded to have I^2Ccommunication with the IC. EN may be connected to control the enable function. Alternatively, it may be left unbonded and subsequently pulled to a logic HIGH via an internal pullup.

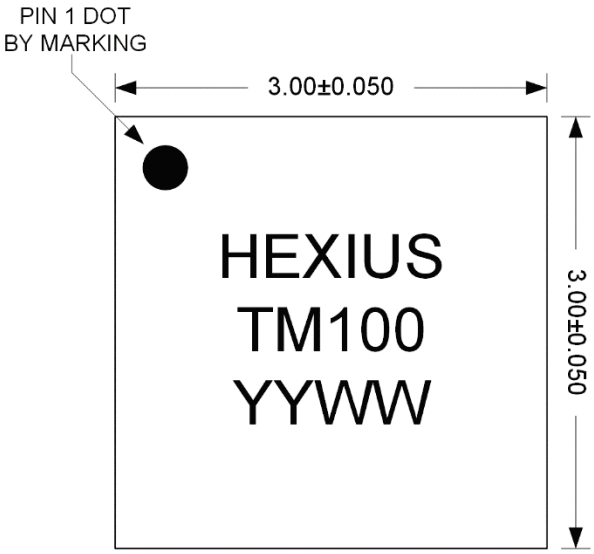
Optional Functionality – Pads 20, 22, 39

XTUNE, THRM & and MUX are pads for optional functionality. XTUNE needs to be bonded if an external varactor is being used. THRM and MUX need to be bonded if the higher-level module circuit uses external signals to be sampled with the ADC. For example, an external thermistor can be connected to THRM for additional temperature measurement.

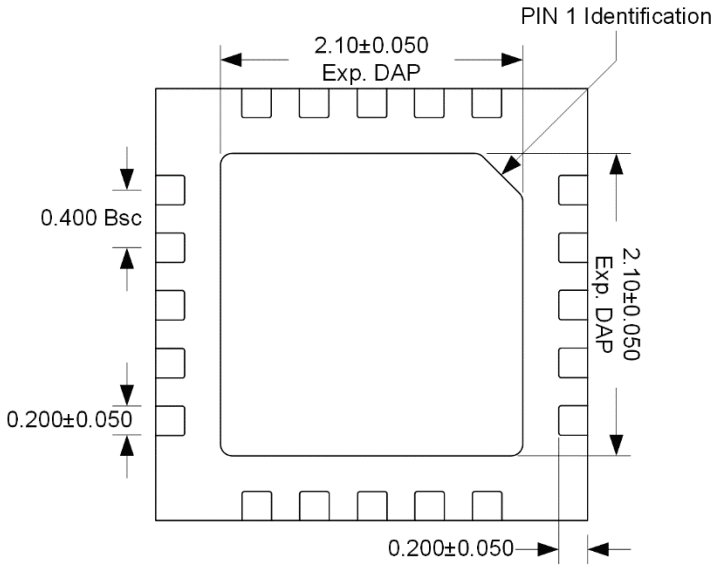
RFOUT Options – Pads 33, 34

The TM100 RFOUT Output Stage has two driver options to produce different edge rates. Depending on the application, one driver can be bonded instead of the other. However, the driver circuits can be bonded together (shorted) and individually selected via the control software. The packaged version of the TM100 shorts pad 33 and 34 to the RFOUT pin.

PACKAGE OUTLINE

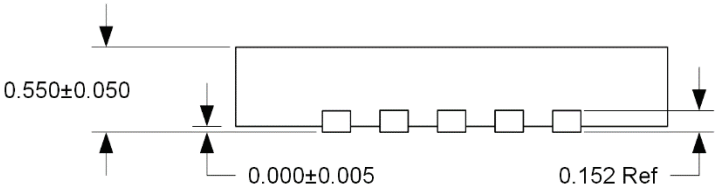


TOP VIEW



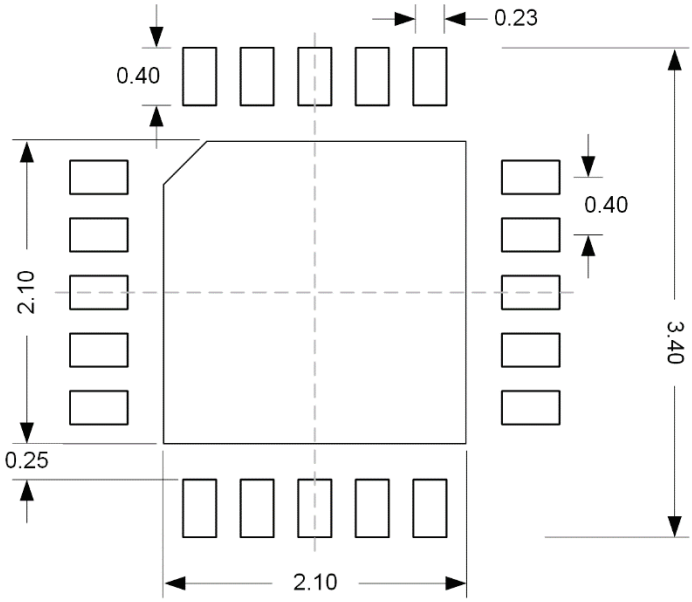
BOTTOM VIEW

All units are in millimeters



SIDE VIEW

PCB LAND PATTERN/FOOTPRINT



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