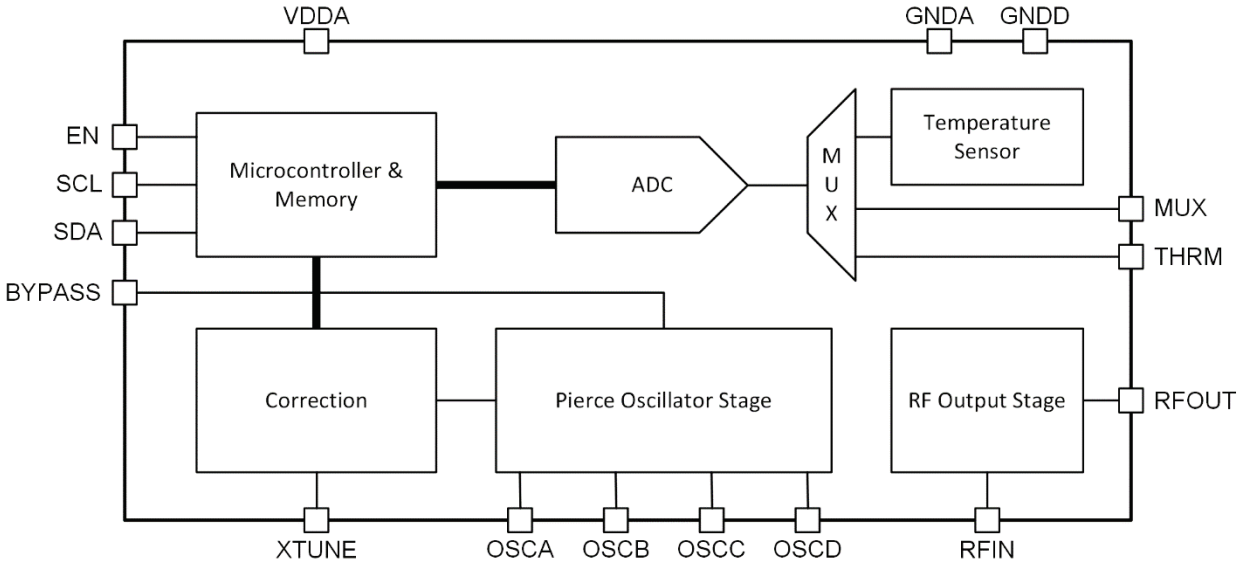
TCXO Thermal Management IC

Description

The TM100 is a fully integrated programmable thermal management unit that monitors, controls, and corrects analog circuitry across a wide temperature range. The TM100 is primarily intended for TCXO applications and includes a temperature sensor, internal Pierce oscillator & output stage and data converters combined with a microcontroller (MCU) and memory structures to run temperature correction programs. The integrated Pierce oscillator and output stage are designed to be flexible with a variety of oscillator and crystal configurations. The TM100 includes many programmable functionality options, and a software package makes it easy to configure and implement customizable crystal correction algorithms. It communicates via an I^2C interface and is available in a 3mm x 3mm package or as die.

Block Diagram



Features

- Low Phase Noise Oscillator
- High accuracy temperature sensor
- Various crystal correction options available
  - Selectable polynomial order curve-fit
  - Lookup tables
- Simple software configuration

Applications

- TCXO Modules

Ordering Information

Order Number	Package	Quantity	RoHS	MSL Rating	Leadframe
TM100-T1	20L STSLP QFN	122 – Tube	Yes	1	NiPdAu
TM100-R1	20L STSLP QFN	1000 – 7” Reel	Yes	1	NiPdAu
TM100-X	Die	Upon Request	n/a	n/a	n/a

SPECIFICATIONS

Environmental Specifications

Table 1 Recommended Operating Conditions

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage	VDDA ± 5%	3.135	3.3	3.465	V
Operating Temperature		-40		125	°C
OTP Programming Temperature		0		50	°C

Internal Temperature Sensor Specifications

Table 2 Temperature Sensor Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Absolute Accuracy		-0.25		0.25	°C
Voltage Range	-40C to 125C	1.32		2.5	V
Resolution	ADC LSB		0.11		°C
Linearity	-40C to 125C		0.6		%
	70C to 125C		0.2		

Oscillator Specifications

Table 3 Oscillator Specifications

Description	Conditions	Min	Typ	Max	Unit
Input Frequency	Internal CA/CB capacitors only	5[1]		155	MHz
CA Range	Adjustable	2		52	pF
CB Range	Adjustable	2		62	pF
RD Range	Adjustable	25		1000	Ω
RF Range	Adjustable	1.6k		100k	Ω
Duty Cycle	Adjustable	45	50	55	%

[1] Using external capacitors allows for operation below 5MHz

Output Specifications

Table 4 Output Stage Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Maximum Output Frequency	15pF load		200		MHz
	50pF load		100		
Rise/Fall Time (10%-90%) of VDDA	8mA drive - 15pF Load		2.0		ns
	8mA drive - 50pF Load		4.8		
	4mA drive - 15pF Load		3.7		
	4mA drive - 50pF Load		9.1		

PIN CONFIGURATION AND FUNCTION

Table 5 TM100 Pinout

Pin	Name	I/O/P	Description
1	OSCD	I/O	Crystal drive when internal Varicap is used.
2	OSCC	I/O	Crystal drive when internal Varicap is bypassed and not used.
3	GNDA	P	Analog ground
4	BYPASS	I/O	Internal oscillator power supply. Will require either 22uF/0.01uF bypass capacitors or 1nF compensation capacitor depending on configuration.
5	GNDD	P	Digital ground
6	SCL	I/O	Tuning (EFC) & I^2C interface input clock. An external pullup resistor to VDDA of 10kΩ is needed during I^2C communications. The pin contains an internal pull-down resistor of 110 kΩ. 5V tolerant.
7	SDA	I/O	Open drain serial data input/output for the I^2C interface. An external pullup resistor to VDDA of 10kΩ is needed during I^2C communications. The pin contains a high value internal pull-down resistor. 5V tolerant.
8	N/C	n/a	Not connected
9	THRM	I	External NTC thermistor input. Use this input to use an external thermistor as an alternative crystal measurement method than the internal IC temperature sensor.
10	XTUNE	I/O	External Tuning Voltage. The pin is driven by the output of the Correction DAC and/or the EFC input. It typically controls the voltage on an external varactor. It is not connected when the Correction block is configured to drive the internal Varicap.
11	EN	I/O	Enable signal. The polarity and default state is programmable through the internal processor. 5V tolerant.
12	N/C	n/a	Not connected
13	GNDA	P	Analog ground
14	RFOUT	O	RF Output. The RFOUT pin provides a CMOS output signal with properties defined in the output stage section.
15	RFIN	I	RF Input. RFIN is the input receiver connection from the oscillator stage output. It is usually driven via a capacitor from OSCB.
16	N/C	n/a	Not connected
17	MUX	I	General purpose input for ADC conversion. Signals on this pin can be sampled, converted to the digital domain, and used as part of the correction/monitoring algorithm. Contact Hexius for use of this pin.
18	VDDA	P	3.3V Analog positive supply. The current on this pin can be up to 20mA.
19	OSCB	I/O	Pierce inverter state output. This signal is usually fed to RFIN via a series capacitance to provide a drive to the output stages.
20	OSCA	I/O	Pierce inverter stage input from crystal.
21	GNDA	P	Analog ground

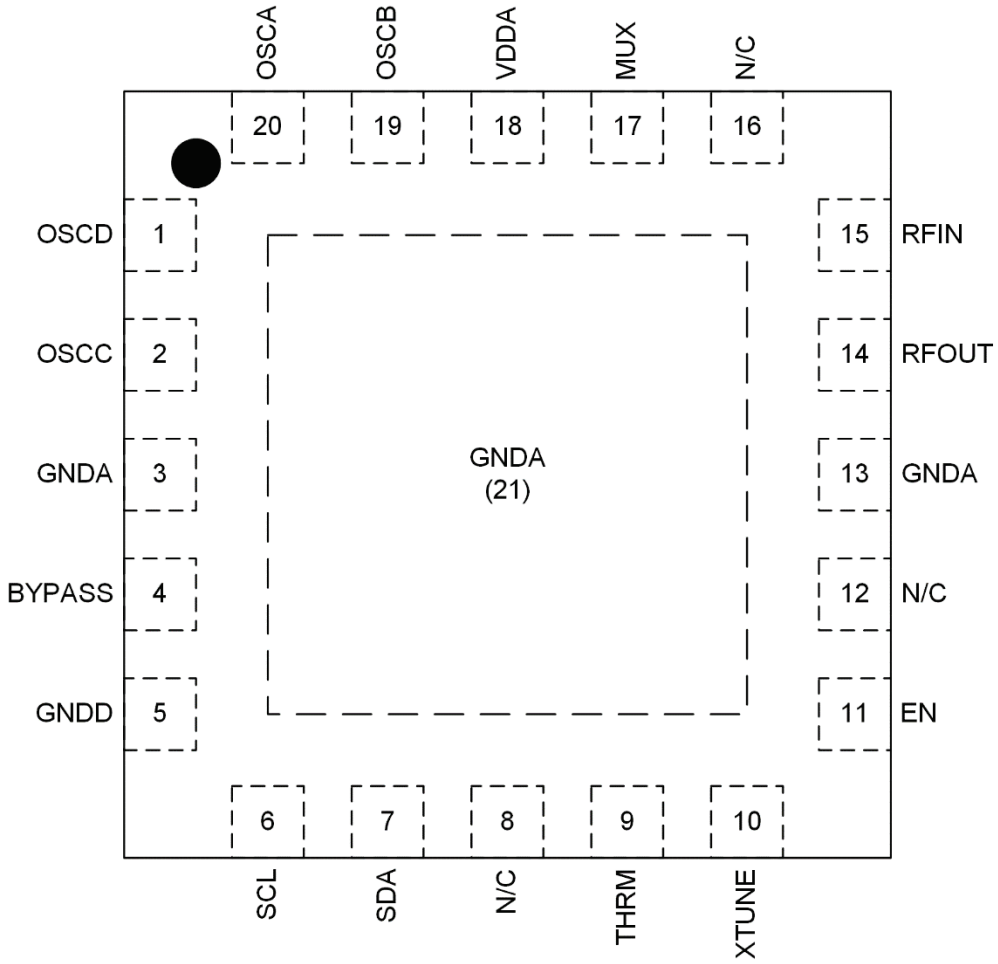


Figure 1 TM100 Package Pinout

BLOCK DESCRIPTION & FUNCTIONALITY

Oscillator Stage

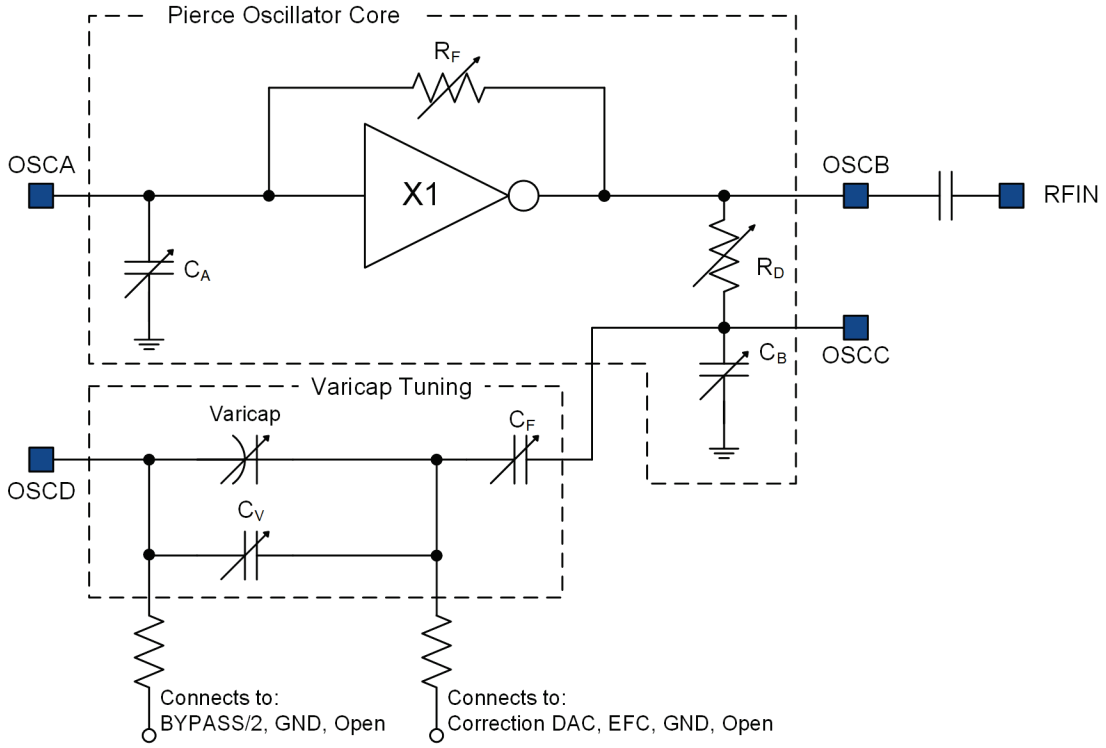


Figure 2 Oscillator Stage Architecture

Pierce Oscillator Core

The oscillator uses a Pierce architecture, designed to be compatible with fundamental or overtone AT cut crystals and overtone SC cut crystals up to 156MHz. It includes an embedded inverter with adjustable resistors and capacitors. The gain stage (X1) is an optimized P/N FET inverter pair. The values for C_A, C_B, C_F, C_V, R_F, and R_D are set using the control registers and are easily configured with the TMx00 Control Software. The oscillator stage is powered through the BYPASS pin and can be shorted to the VDDA pin of the IC or decoupled from VDDA by configuring an internally 2.9V regulator to drive the BYPASS pin. See the Application Notes more information.

Most oscillator applications can be met with the internal component value selections, thereby reducing the amount external components needed to construct an oscillator. Alternatively, the R_F and R_D select logic allows disabling the internal resistors for use with external components. C_A and C_B capacitors can be fully disabled especially for applications with matching and trap networks in series with overtone crystals. When the C_A and C_B capacitors are disabled, the minimum capacitance is ~2pF.

Oscillator Connections

OSCA is the Pierce inverter input, typically connected to one side of the crystal. OSCB is the Pierce inverter output used to feed an output stage. OSCA and OSCD are the crystal connections for applications that use the internal Varicap. A blocking cap is necessary between OSCC or OSCD and the crystal to prevent DC bias across the crystal. For applications that use an external varactor, the other side of the crystal is connected to OSCC and OSCD is left open.

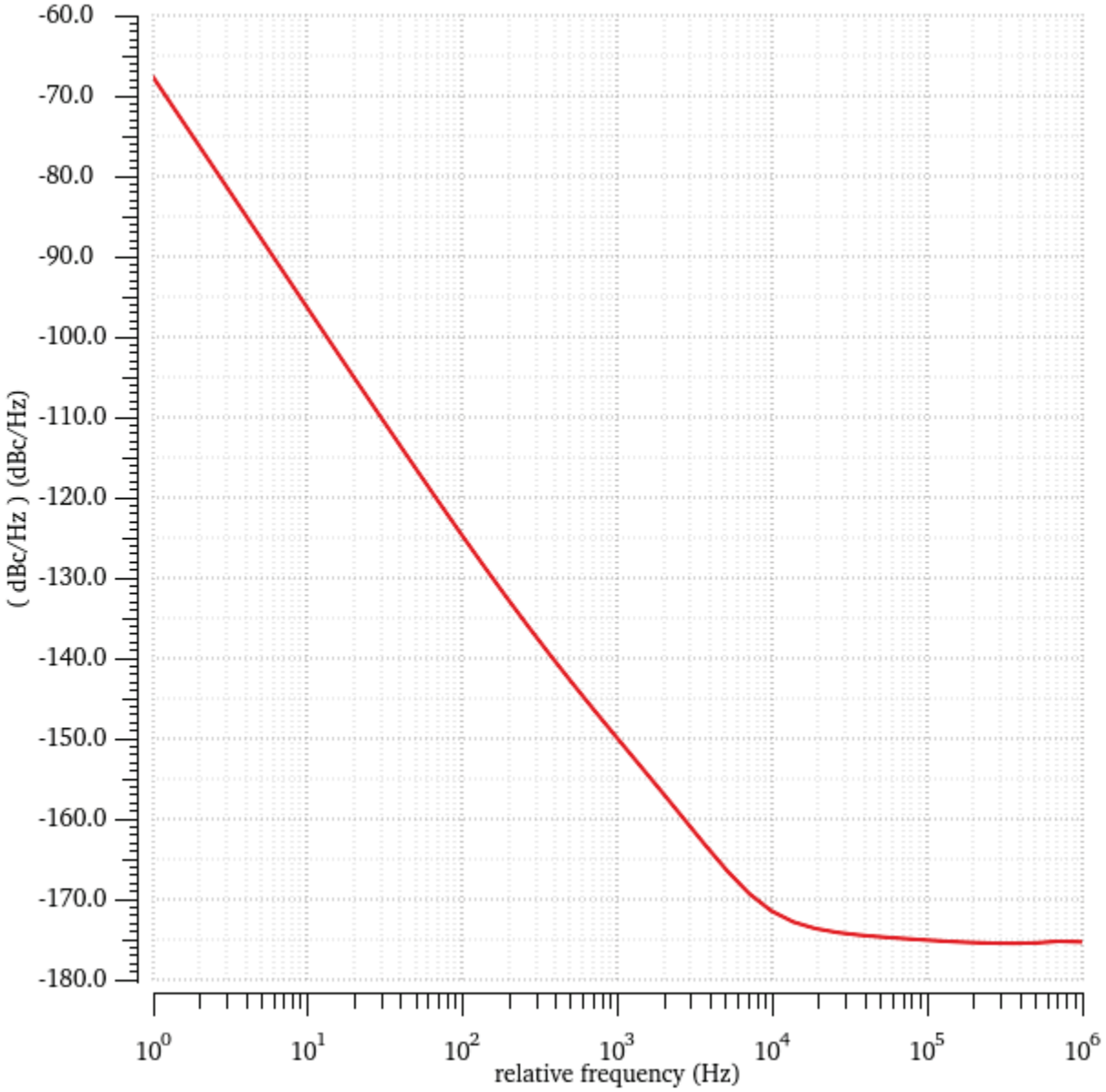


Figure 3 - 20MHz Fundamental, AT-Cut, Internal Varicap Phase Noise

Correction System

The correction system is designed to correct the frequency shifts of a crystal across temperature (Beckman Curve) with either the TM100's internal Varicap or an external varactor. Using the ADC to convert temperature sensor data, the MCU provides the input code to a 12-bit DAC with an output voltage that adjusts the internal Varicap or external varactor to correct crystal frequency variation across temperature.

The correction system uses either the internal Varicap or an external varactor to provide the appropriate crystal pull. The internal Varicap is suitable for low-cost designs that require minimal components. For higher performance requirements, an external varactor may be used and controlled with the XTUNE pin. Please refer to the Oscillator Design Examples and TCXO Design Examples for more information.

The internal Varicap or XTUNE pin can also be controlled from the dual use SCL (EFC) pin via an analog connection. Alternately the EFC or MUX pin can be used as an input to the ADC. The digitized value is processed in the MCU via correction algorithms and fed out via the correction DAC to control the internal Varicap or external varactor.

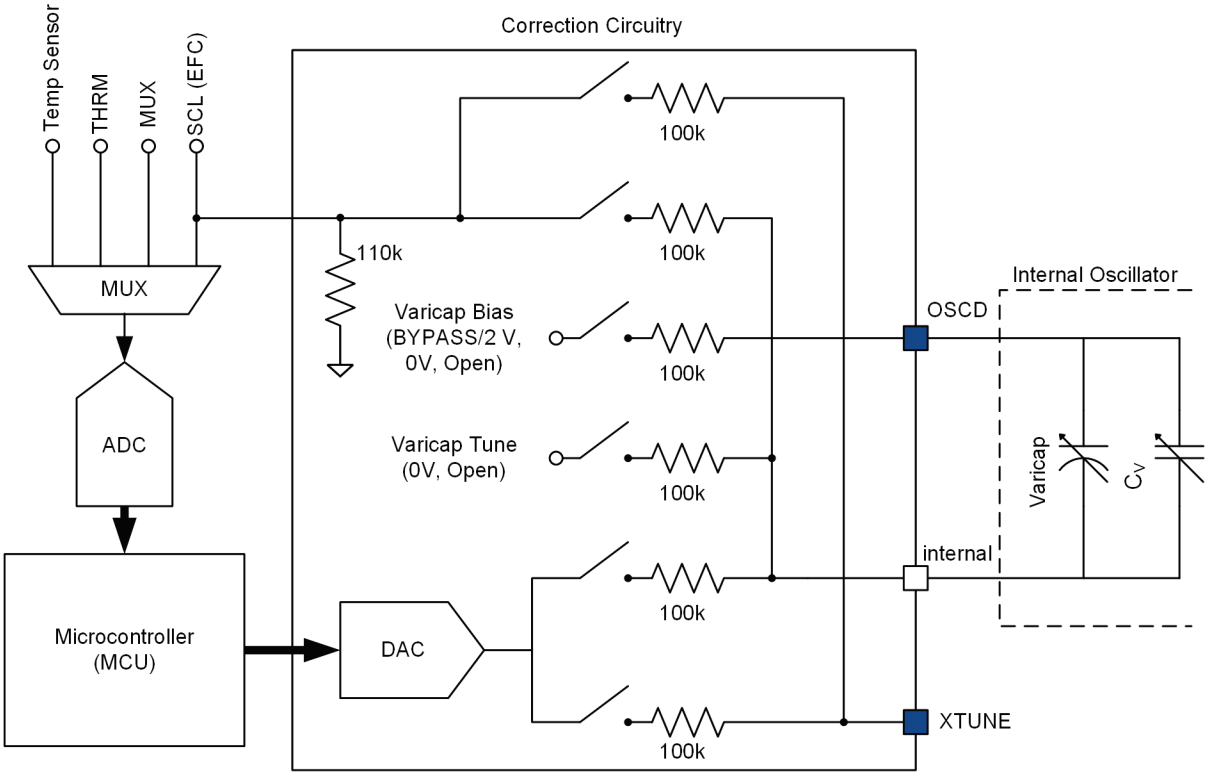


Figure 4 Correction System Diagram

TCXO Temperature Correction Algorithm Overview

The TM100 supports three correction algorithms to compensate for temperature and voltage non-idealities:

1. **Lookup Table** – Temperature correction algorithm
2. **Temperature Polynomial Curve Fit** – Temperature correction algorithm
3. **Supply Voltage Curve Fit** – Voltage correction algorithm

The TMx00 correction algorithms use integer numbers (digital codes) that represent temperatures and voltages to make compensation adjustments. The ADC converts analog signals into the digital domain for the MCU to calculate the appropriate Correction DAC input code and produce an analog correction voltage.

The first two algorithms use a *Temp Code* input to generate a *CorrDAC Code* from the Correction DAC output to correct frequency variations over temperature. Only one of the temperature correction algorithms may be used during operation.

The *Temp Code* value is an integer with the range of 0 to 4095 and corresponds to the temperature being measured and digitized through the ADC. A -40C to 90C temperature range will utilize a *Temp Code* range of approximately 2000 to 3200. The *Temp Code* is produced from either the IC internal temperature sensor or an external thermistor (via the THRM pin).

The *CorrDAC Code* value is an integer with the range of 0 to 4095 and corresponds to the DAC input code needed to vary the capacitance across an external varactor or the internal TMx00 Varicap to correct the frequency variation for a given temperature.

The *CorrDAC Voltage* is resulting Correction DAC output voltage for a given *CorrDAC Code*. It is calculated by multiplying the Correction DAC's reference voltage by the ratio of the *CorrDAC Code* to the Correction DAC's full-scale code (4095).

$$CorrDAC\ Voltage = \frac{CorrDAC\ Code}{4095} * BYPASS\ Pin\ Voltage$$

As a brief relationship example, a measured temperature of 25C may produce a *Temp Code* of 2541 and results in a *CorrDAC Code* of 1983 and a *CorrDAC Voltage* of 1.4043V for the correct center frequency of a unique TCXO assembly.

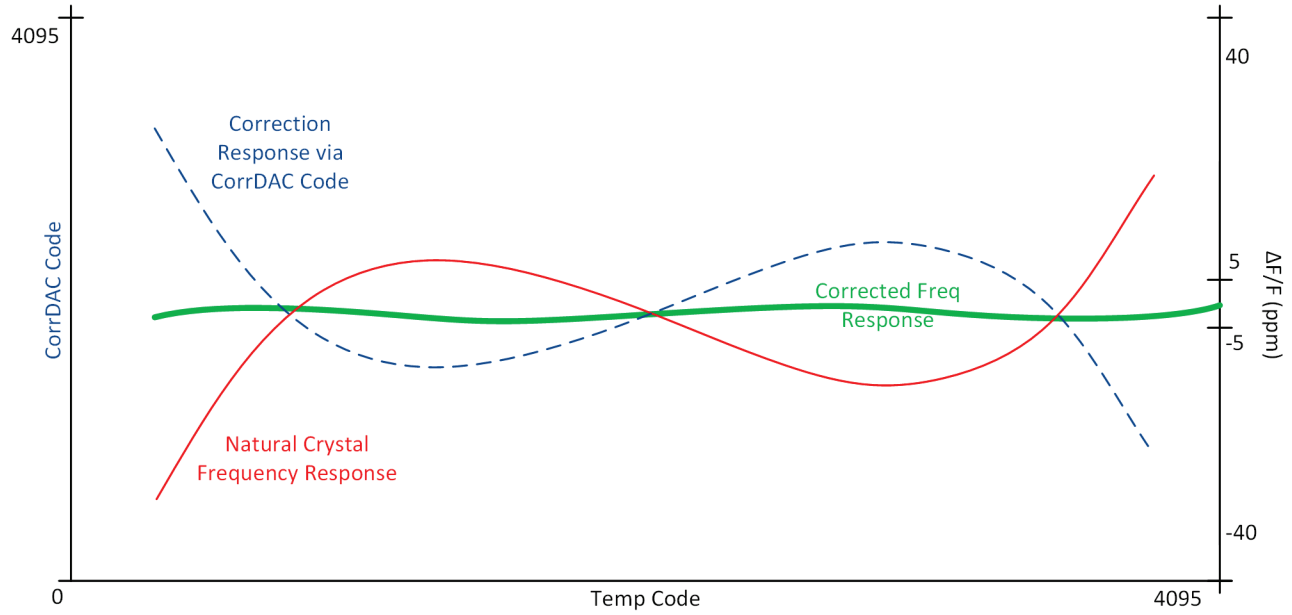
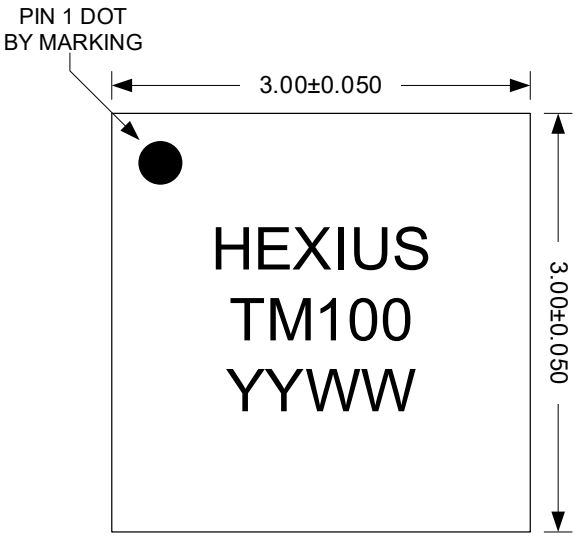
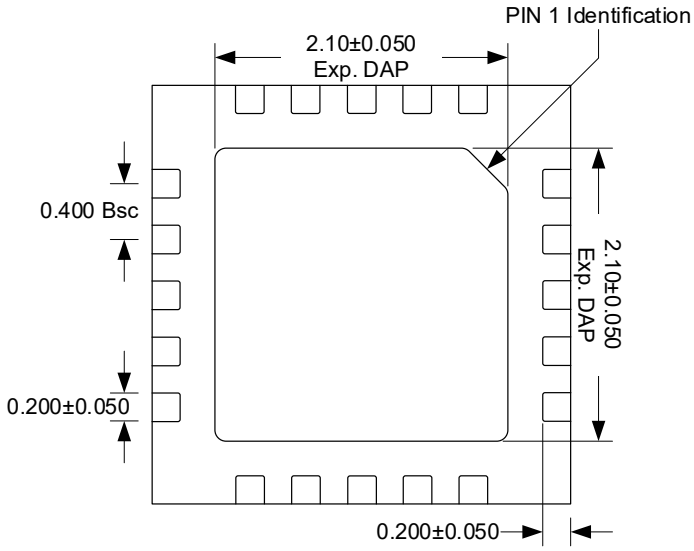


Figure 5 Temp Code and CorrDac Code Relationship

PACKAGE OUTLINE

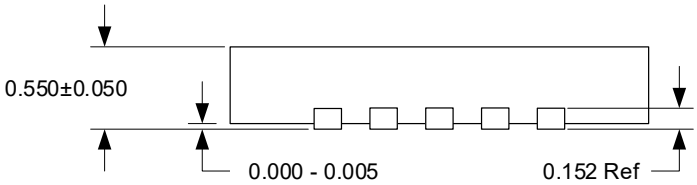


TOP VIEW



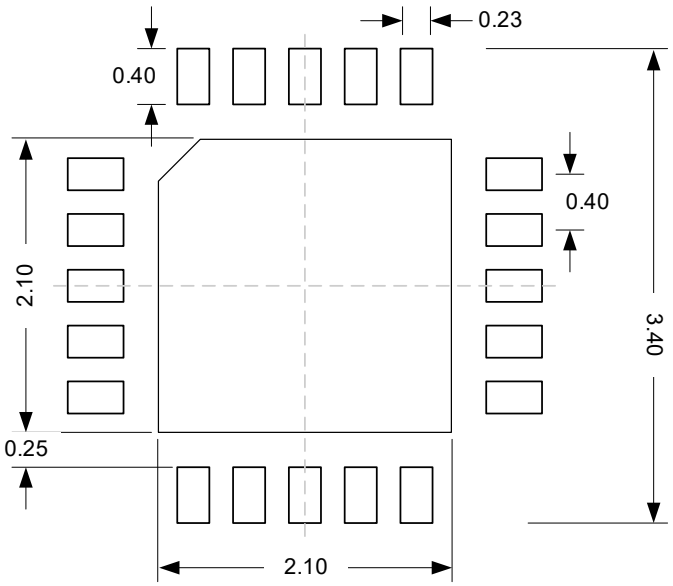
BOTTOM VIEW

All units are in millimeters



SIDE VIEW

PCB LAND PATTERN/FOOTPRINT



For more information about all Hexius Semiconductor products visit our website at

www.hexiussemi.com