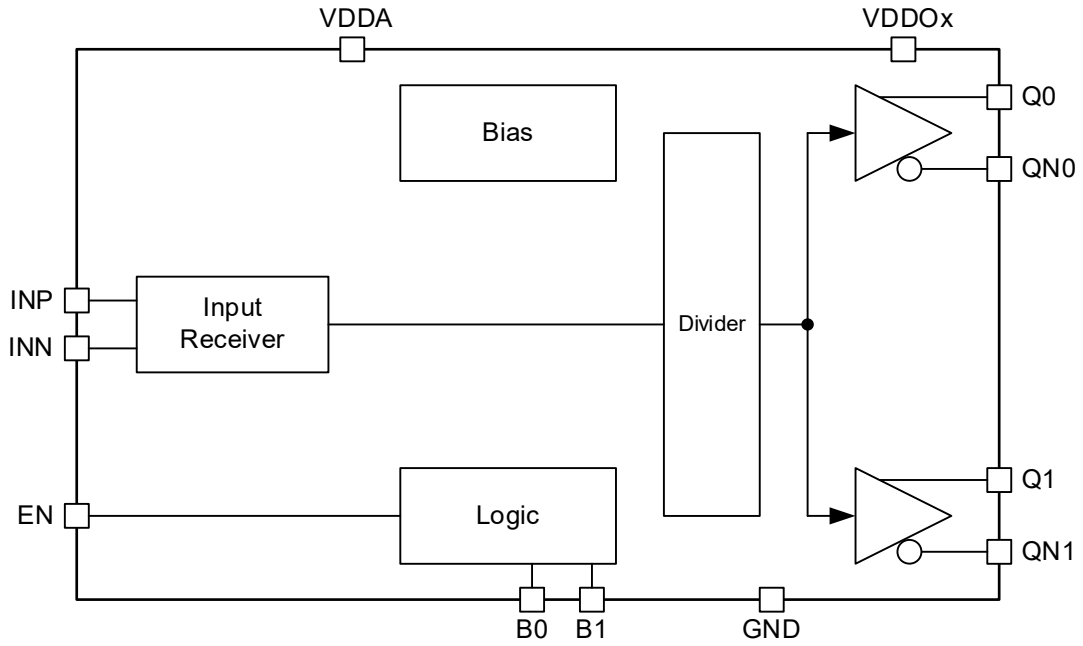
1:2 LVPECL Fanout Buffer & Divider

DESCRIPTION

The CF112P is an extremely low additive jitter 1:2 LVPECL clock fanout and divider. Its sensitive differential input receiver accepts low amplitude sinewave, CMOS, LVPECL, LVDS, CML, and HCSL signals to perform LVPECL output logic level translation, signal fanout, and configurable frequency division (or passthrough) up to 1000MHz. The CF112P is designed to meet extremely low additive jitter and skew requirements operating in an extended temperature range. The divide functionality (or passthrough) is configured with static voltages to external control pins.

BLOCK DIAGRAM



FEATURES

- Input signal sensitivity down to 30mVpp
- Input/output signal frequency up to 1000MHz
- Additive Jitter <20fs @ 1GHz, <40fs @ 156MHz
- 30ps output to output skew
- Configurable output divider
- Extended Temp Range -55°C to 125°C

APPLICATIONS

- 5G/6G clock distribution
- Low jitter clock trees
- Logic translation & signal restoration
- Wired & wireless communications
- Microprocessor clock distribution
- High Speed ADC, DAC clock driver

ORDERING INFORMATION

Order Number	Package	Form	Quantity	RoHS	MSL Rating	Leadframe
CF112P-T1	16L TSLP QFN	Tube	123	Yes	1	NiPdAu
CF112P-R1	16L TSLP QFN	7” Reel	1000	Yes	1	NiPdAu

TABLE OF CONTENTS

REVISION HISTORY

Revision	Date	Description
1.0	5/2023	Initial Release

SPECIFICATIONS

Recommended Operating Conditions

Table 1 Recommended Operating Conditions

Parameter	Conditions	Min	Typ	Max	Unit
Supply Voltage	±10%	2.97	3.3	3.63	V
Operating Temperature		-55	27	125	°C

DC Specifications

Table 2 DC Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Analog Supply Current (VDDA)	156MHz Sinewave Input Signal		17		mA
	1GHz Sinewave Input Signal		33		
Output Driver Supply Current Per VDDOx Supply Pin	156MHz Sinewave Input Signal		49		mA
	1GHz Sinewave Input Signal		54		
Control Logic HIGH(1) Input Voltage	Pins - B0 / B1 / EN	0.9*VDDA			V
Control Logic OPEN Input Voltage	Pins - B0 / B1		OPEN		
Control Logic LOW(0) Input Voltage	Pins - B0 / B1 / EN			0.1*VDDA	

Input Signal Specifications

Table 3 Input Signal Specifications

Parameter	Conditions		Min	Typ	Max	Unit
Input Signal Slew Rate			0.5			V/ns
Input Signal Amplitude	Single ended input - Input signal biased at VDDA/2	156MHZ	-26			dBm
		500MHZ	-22			
		1GHz	-13			
Maximum Input Frequency	Divide by 1 (passthrough)				1000	MHz
	Divide by 2,4,8,16,32				750	

LVPECL Output Specifications

Table 4 LVPECL Output Specifications

Parameter	Conditions	Min	Typ	Max	Unit
Output Voltage Level	Output High Voltage (V_{OH}) - 100Ω DC load	VDDOx-1.15			V
	Output Low Voltage (V_{OL}) - 100Ω DC load			VDDOx-1.75	
Single Ended Voltage Swing	100Ω DC load	0.74			V
Output Frequency				1000	MHz
Output Rise/Fall Time	156MHz, 90%-10% - 150Ω DC load		6.45		ns
Additive Jitter	155MHz, 12kHz-20MHz Integration		40		fs
	1GHz, 12kHz-20MHz Integration		20		
Propagation Delay		1.3		2.5	ns
Output to Output Skew	Differential output through balun, 100Ω DC load		30	50	ps

Absolute Maximum Ratings

Table 5 Absolute Maximum Ratings

Parameter	Conditions	Min	Max	Unit
Supply Voltage	VDDA & VDDOx	-0.5	3.8	V
Input Voltage	INP / INN	-0.5	3.8	V
Output Voltage	Qx / QNx	-0.5	3.8	V
Soldering Temperature	Packaging application		260	°C
Storage Temperature		-55	150	°C
Junction Temperature			150	°C
ESD Ratings	Human Body Model	2000		V
	Machine Model	100		
	Charged Device Model	1000		

PIN CONFIGURATION AND FUNCTION

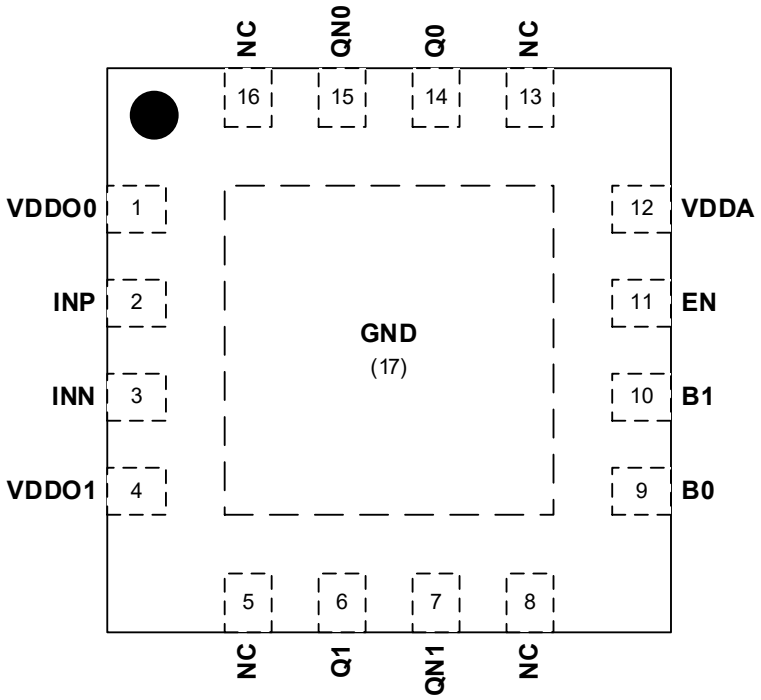


Figure 1 Package Pinout

Table 6 Pin Description

Pin	Name	I/O/P	Description
1	VDDO0	P	Output Driver Power Supply 0. The current on this pin can be up to 60mA
2	INP	I	Positive Differential Input
3	INN	I	Negative Differential Input
4	VDDO1	OP	Output Driver Power Supply 1. The current on this pin can be up to 60mA
5	NC	n/a	Not Connected
6	Q1	O	Output Signal 1
7	QN1	O	Output Signal 1 Complement
8	NC	n/a	Not Connected
9	B0	I	Static Configuration Bit. This pin has three possible input levels: HIGH(1), LOW(0) or OPEN
10	B1	I	Static Configuration Bit. This pin has three possible input levels: HIGH(1), LOW(0) or OPEN
11	EN	I	Enable signal. When EN is connected HIGH, the outputs are enabled. When EN is connected LOW, the outputs are disabled and held in tri-state.
12	VDDA	P	Analog Power Supply. Bypass capacitors of 22uF and 0.01uF values should be connected as close to the IC as possible.
13	NC	n/a	Not Connected
14	Q0	O	Output Signal 0
15	QN0	O	Output Signal 0 Complement
16	NC	n/a	Not Connected
17	GND	P	Ground

BLOCK DESCRIPTION & FUNCTIONALITY

Input Receiver

The input receiver of the CF112P is a very sensitive differential pair input architecture designed for low noise interfacing to sinewave and small amplitude signals as low as 30mVpp (-26dBm) at 156MHz and 140mVpp (-13dBm) at 1GHz. The input receiver minimizes duty cycle degradation of the incoming signal for optimal phase noise performance. For best performance, an input signal slew rate of at least 0.5V/ns is recommended. Logic levels such as LVPECL, CMOS, LVDS, CML, and HCSL interface directly or with common termination architectures (see Application Notes). The CF112P accepts single ended or differential inputs. Differential inputs are recommended for input signals above 750MHz.

Divider

The divider circuitry accepts the input signal and generates a ÷1 (passthrough), 2, 4, 8, 16, or 32 divide ratio based on the static control bit levels. B1 and B0 function as tri-level configuration bits to set the divider value. They can be set to logic LOW(0), logic HIGH(1), or unconnected (OPEN) for the desired frequency division. The divider circuit generates copies of the resulting signal and provides each output stage with the same signal frequency. If different frequencies are needed per output, consider using other Hexius Semiconductor's smaller fanout parts.

Table 7 Divider Value (B1:B0) Functional Definition

Pins	Value	Functional Definition
B1:B0	0:0	÷ 1
	0:1	÷ 2
	1:0	÷ 4
	1:1	÷ 8
	0:OPEN	÷ 16
	1:OPEN	÷ 32
	OPEN:0	÷ 32
	OPEN:1	÷ 32
	OPEN:OPEN	test mode / not used

Output Drivers

The output driver is a current drive topology to maximize switching speed. Approximately 21.1mA of current flows through an output high level pin and 5.1mA of current flows through an output low level pin. The resultant current steering generates the proper LVPECL voltage swing across the two ~100Ω -150Ω external load resistors. Both Q and QN should always be terminated identically to avoid waveform distortion and circulation current caused by unsymmetrical loads. This also applies if only one output pin is being used.

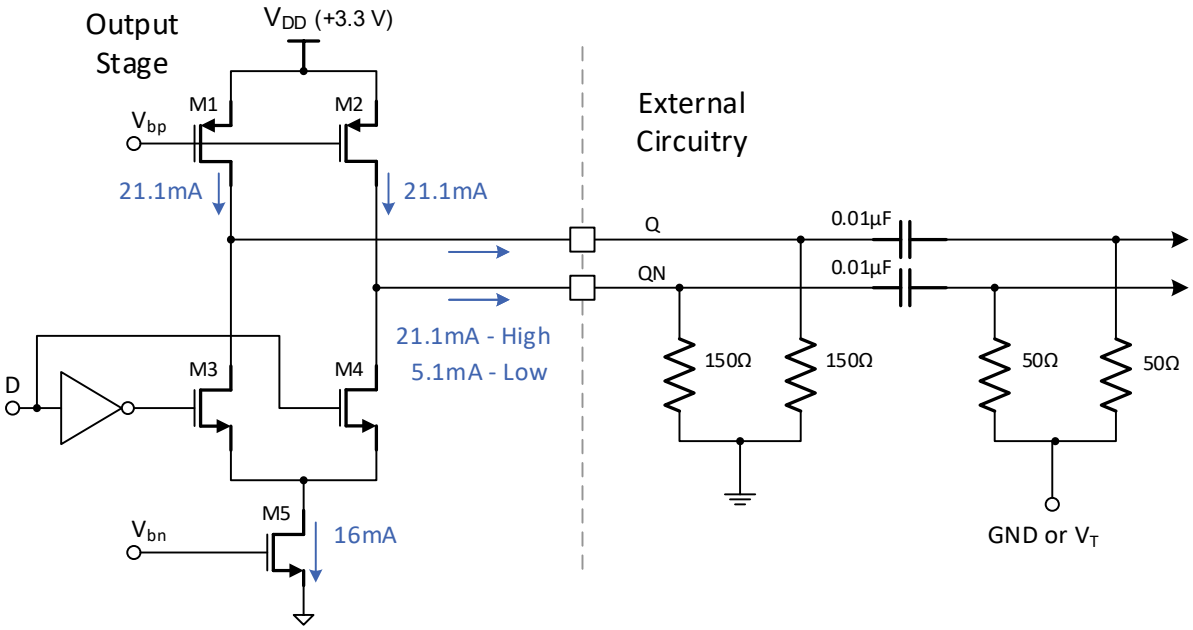


Figure 2 Output Functional Diagram

The EN pin controls the operation of the output stage only. When EN is LOW(0), the outputs are disabled and are put into a tri-state mode but the remaining circuitry of the CF112P is active. When EN is HIGH(1), the outputs are enabled. The EN pin has an internal pull-up that causes the signal to remain HIGH(1) when it is not connected.

Table 8 Enable (EN) Functional Description

Pin	Value	Functional Definition
EN	LOW(0)	Outputs Disabled - Tri-state mode
	HIGH(1)	Outputs Enabled
	OPEN	Outputs Enabled

ADDITIVE JITTER

Definition

The jitter performance of the CF112P is characterized by additive jitter. Additive jitter is the jitter the device adds to a jitter-free clock source as it passes through the device. Additive jitter is random and is not correlated to the jitter of the input clock signal. It is also important to note that the noise of a clock signal (random variation in phase) is defined as phase noise in the frequency domain and jitter in the time domain. The additive jitter is determined by integrating the area under the phase noise curve for a given limit (typically 12kHz-20MHz).

The square of the resultant random RMS jitter at the output is equal to the sum of the squares of the various random RMS jitter sources including: input clock jitter; additive jitter of the buffer; and additive jitter due to power supply noise. There may be additional deterministic jitter sources that are not shown.

The CF112P is not intended to filter clock jitter (clock cleaner).

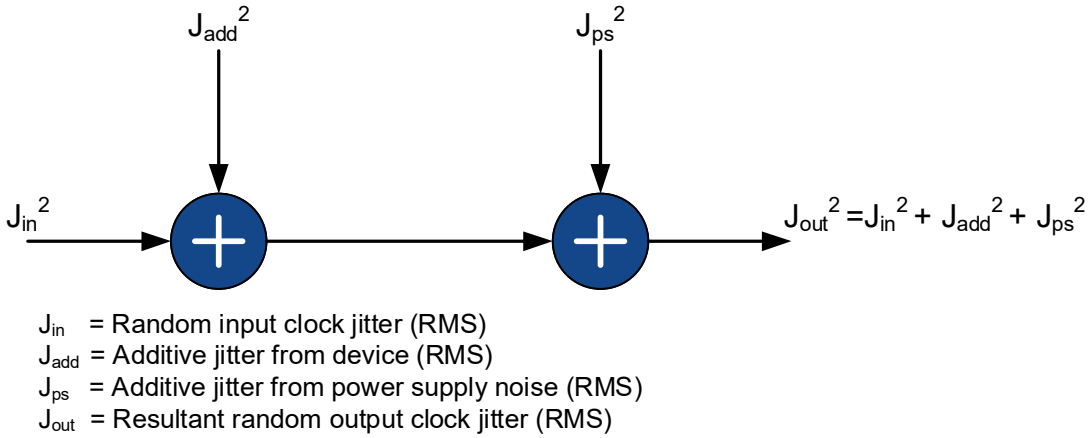


Figure 3 Additive Jitter

Additive Jitter Measurement

To measure the additive jitter of the CF112P, a Holzworth HA7062C and a pair of HX5100 Phase Shifters are used in the configuration illustrated below. Additive phase noise of components and subcomponents give valuable insights to the overall system performance. While absolute phase noise (oscillator or LO noise) can provide the user with the overall performance of a source or total system, additive phase noise focuses the noise contributions of individual elements. The results can help to troubleshoot or predict overall system performance.

Using the HA7062C and HX5100 Phase Shifters, the Holzworth software fully automates setting the quadrature and calibration between the LO and RF input for accurate and repeatable measurements.

For more information regarding the techniques and theory behind this test, please visit Holzworth Instrumentation at holzworth.com.

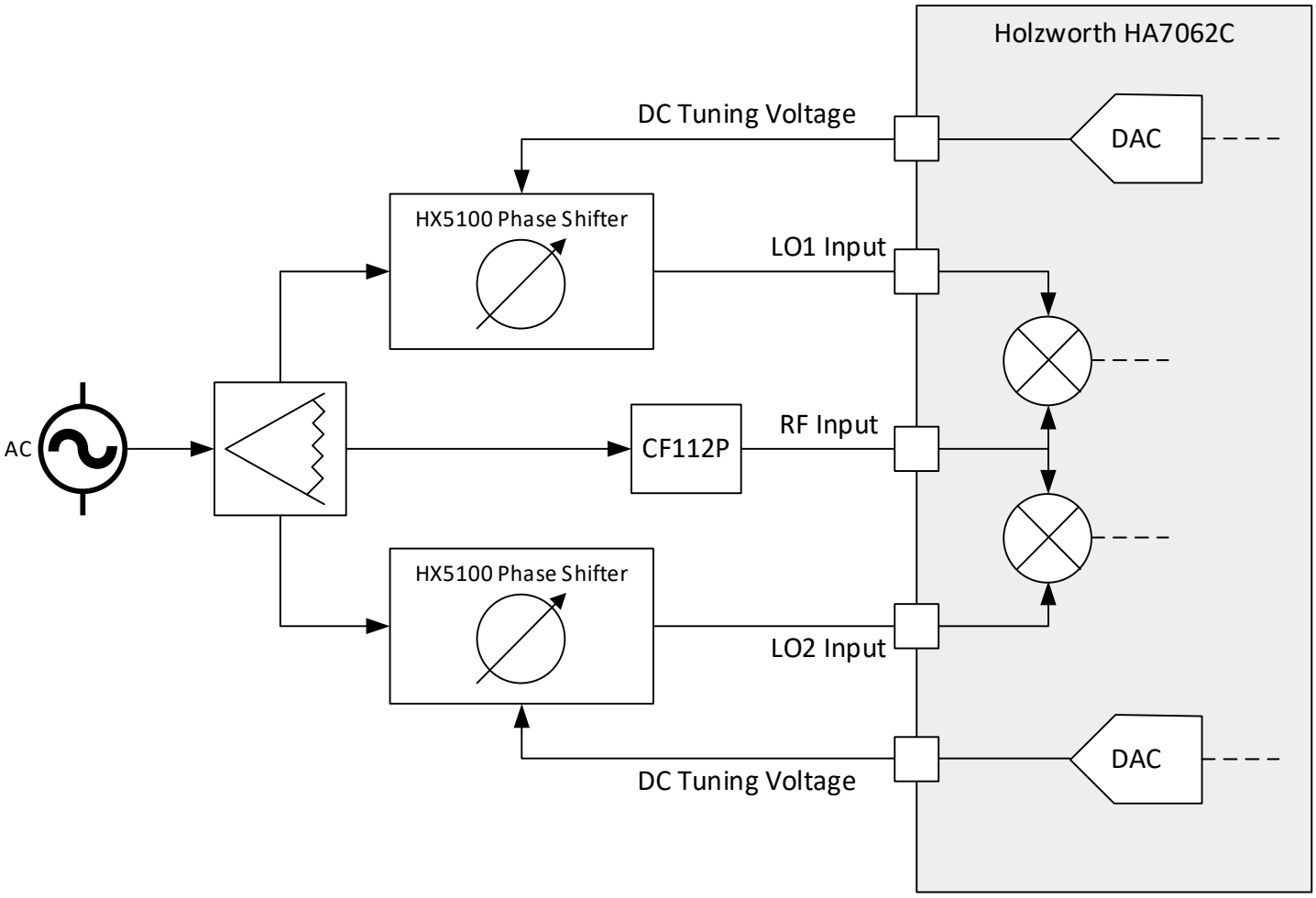
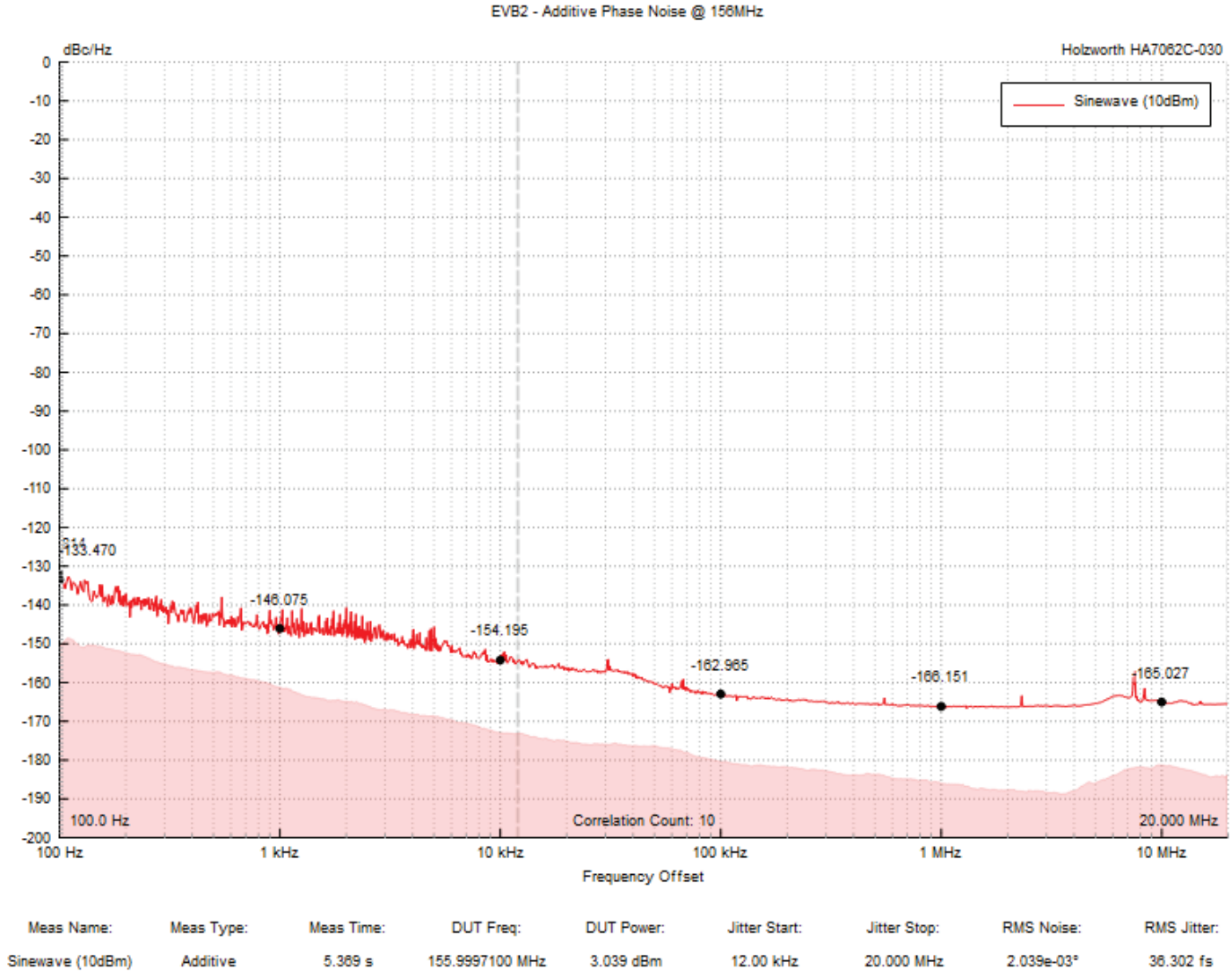


Figure 4 Additive Jitter Measurement Setup

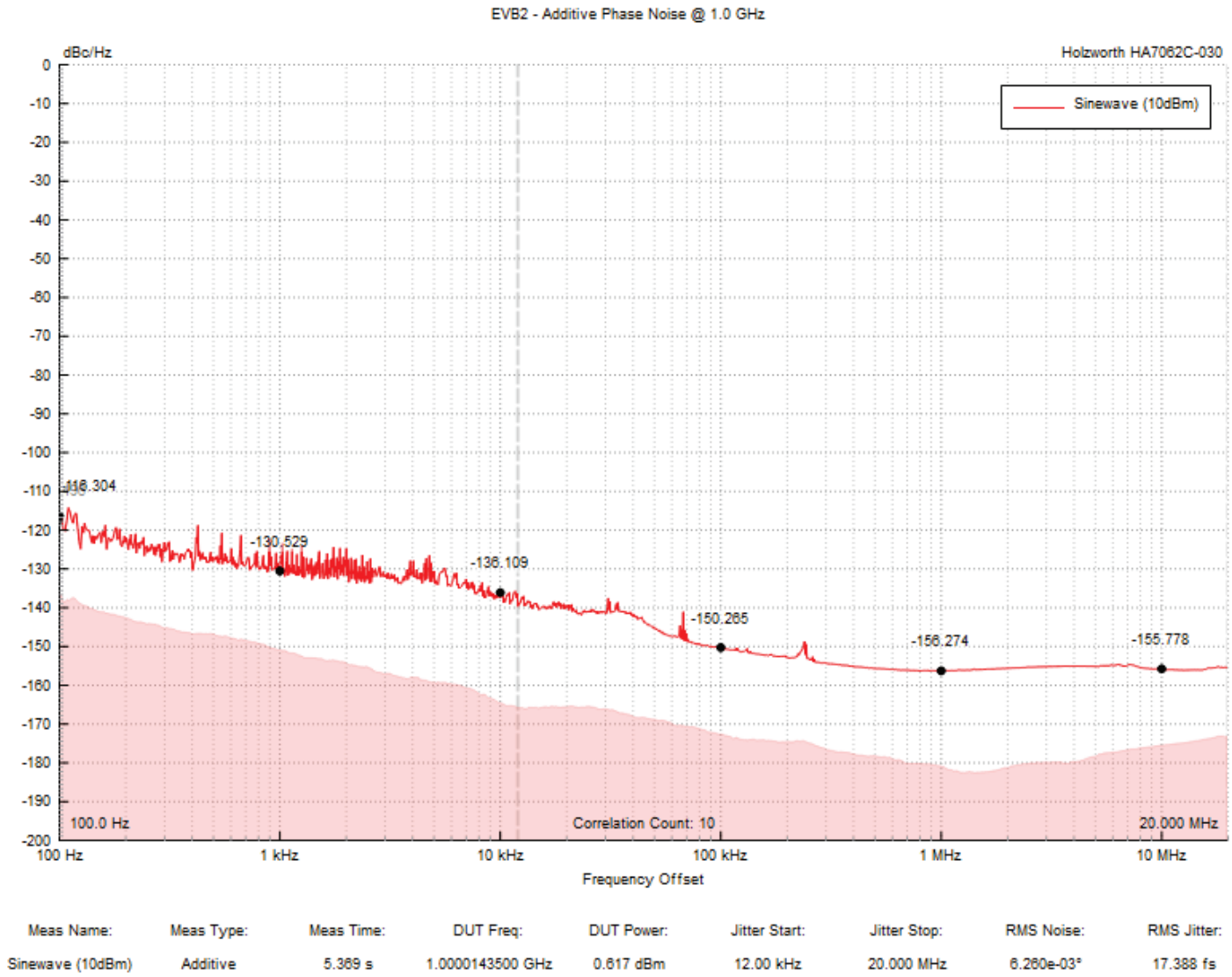
PERFORMANCE

Typical Phase Noise and Additive Jitter Performance



Meas Name:	Meas Type:	Meas Time:	DUT Freq:	DUT Power:	Jitter Start:	Jitter Stop:	RMS Noise:	RMS Jitter:
Sinewave (10dBm)	Additive	5.369 s	155.9997100 MHz	3.039 dBm	12.00 kHz	20.000 MHz	2.039e-03°	36.302 fs

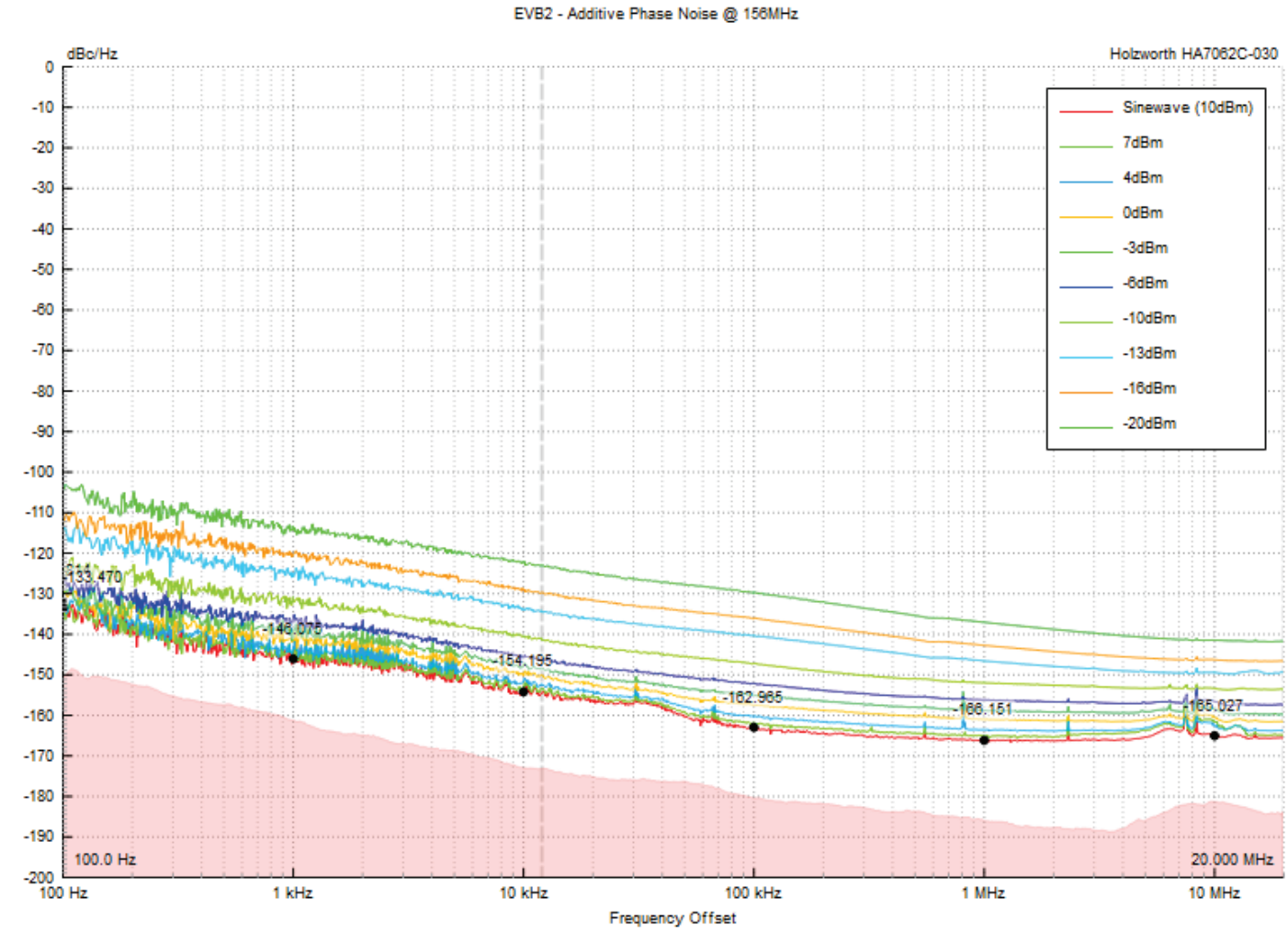
Figure 5 Typical Phase Noise and Additive Jitter Performance with 156MHz Sinewave Input



Meas Name:	Meas Type:	Meas Time:	DUT Freq:	DUT Power:	Jitter Start:	Jitter Stop:	RMS Noise:	RMS Jitter:
Sinewave (10dBm)	Additive	5.369 s	1.0000143500 GHz	0.617 dBm	12.00 kHz	20.000 MHz	6.260e-03°	17.388 fs

Figure 6 Typical Phase Noise and Additive Jitter Performance with 1GHz Sinewave Input

Phase Noise & Additive Jitter vs. Input Signal Amplitude



Meas Name:	Meas Type:	Meas Time:	DUT Freq:	DUT Power:	Jitter Start:	Jitter Stop:	RMS Noise:	RMS Jitter:
Sinewave (10dBm)	Additive	5.369 s	155.9997100 MHz	3.039 dBm	12.00 kHz	20.000 MHz	2.039e-03°	36.302 fs

Figure 7 Phase Noise vs Input Signal Amplitude with 156MHz Sinewave Input

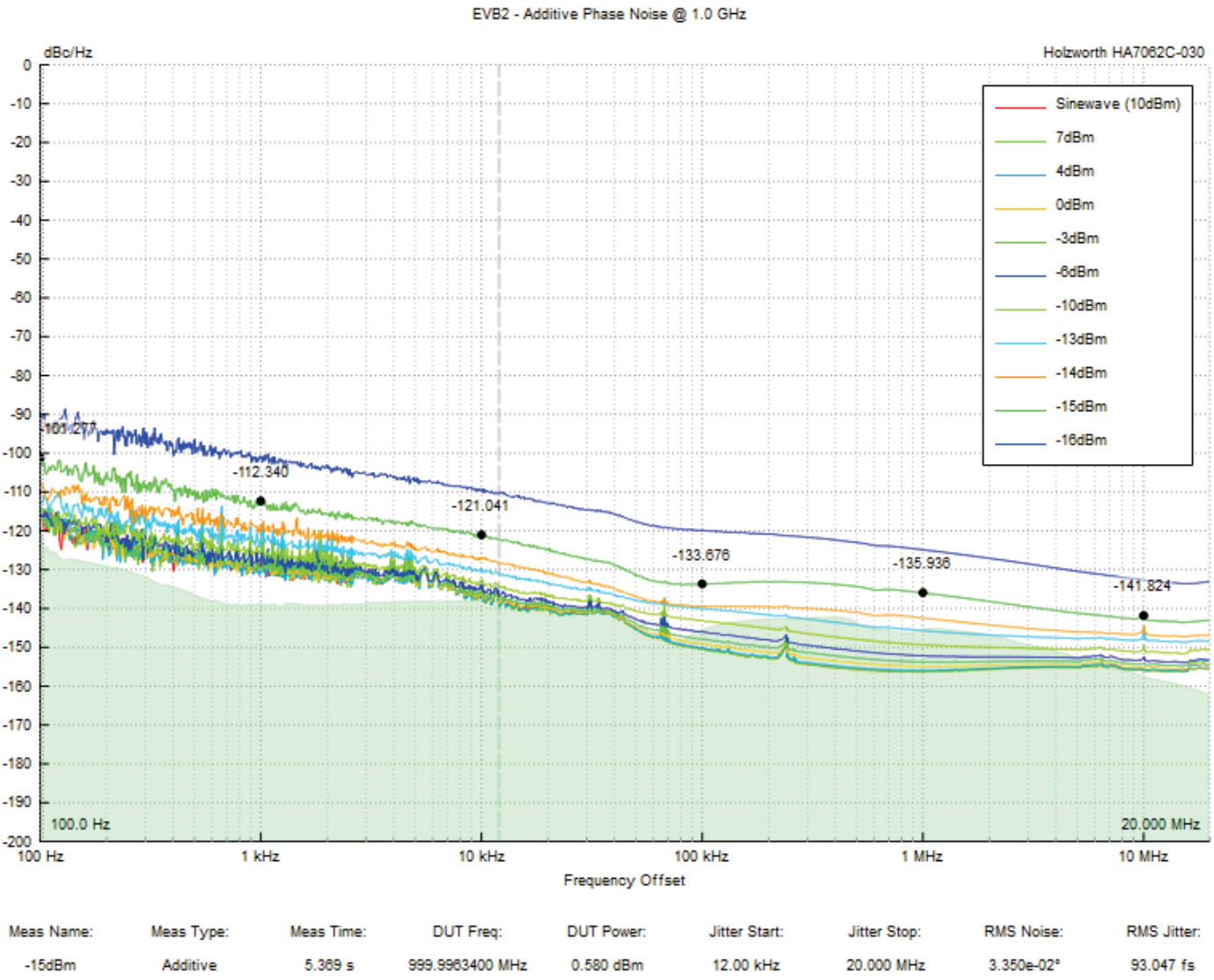


Figure 8 Phase Noise vs Input Signal Amplitude with 1GHz Sinewave Input

Table 9 Additive Jitter vs Input Signal Amplitude – 156MHz

Input Amplitude (dBm)	Additive Jitter (fs RMS)
13	36.30
10	43.85
7	46.06
3	58.18
0	72.02
-3	92.88
-7	143.28
-10	238.32
-13	350.26
-17	643.11

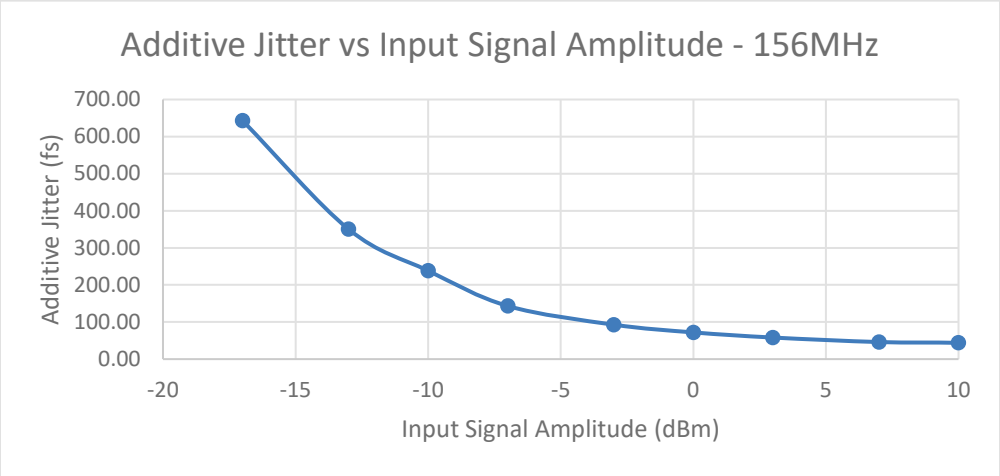
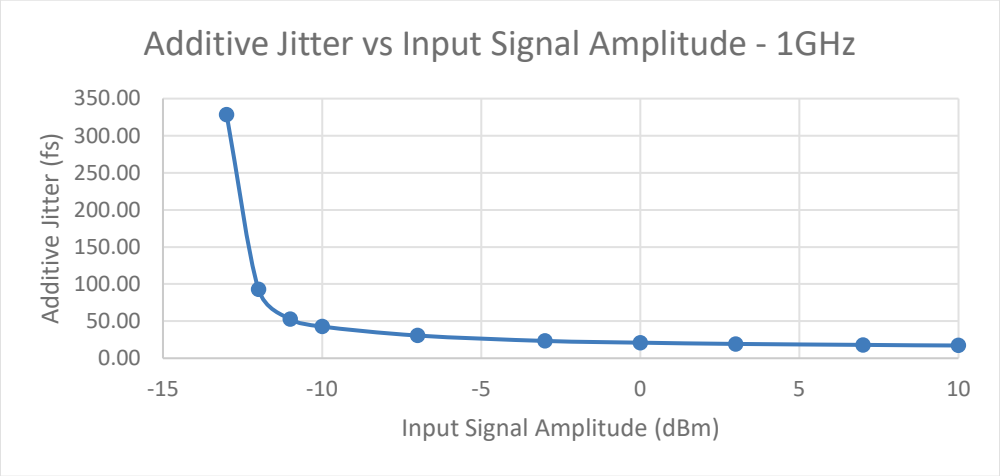


Table 10 Additive Jitter vs Input Signal Amplitude – 1GHz

Input Amplitude (dBm)	Additive Jitter (fs RMS)
13	17.39
10	17.18
7	18.02
3	19.31
0	21.00
-3	23.34
-7	30.60
-10	42.73
-11	52.75
-12	93.05
-13	328.47



Output Waveforms

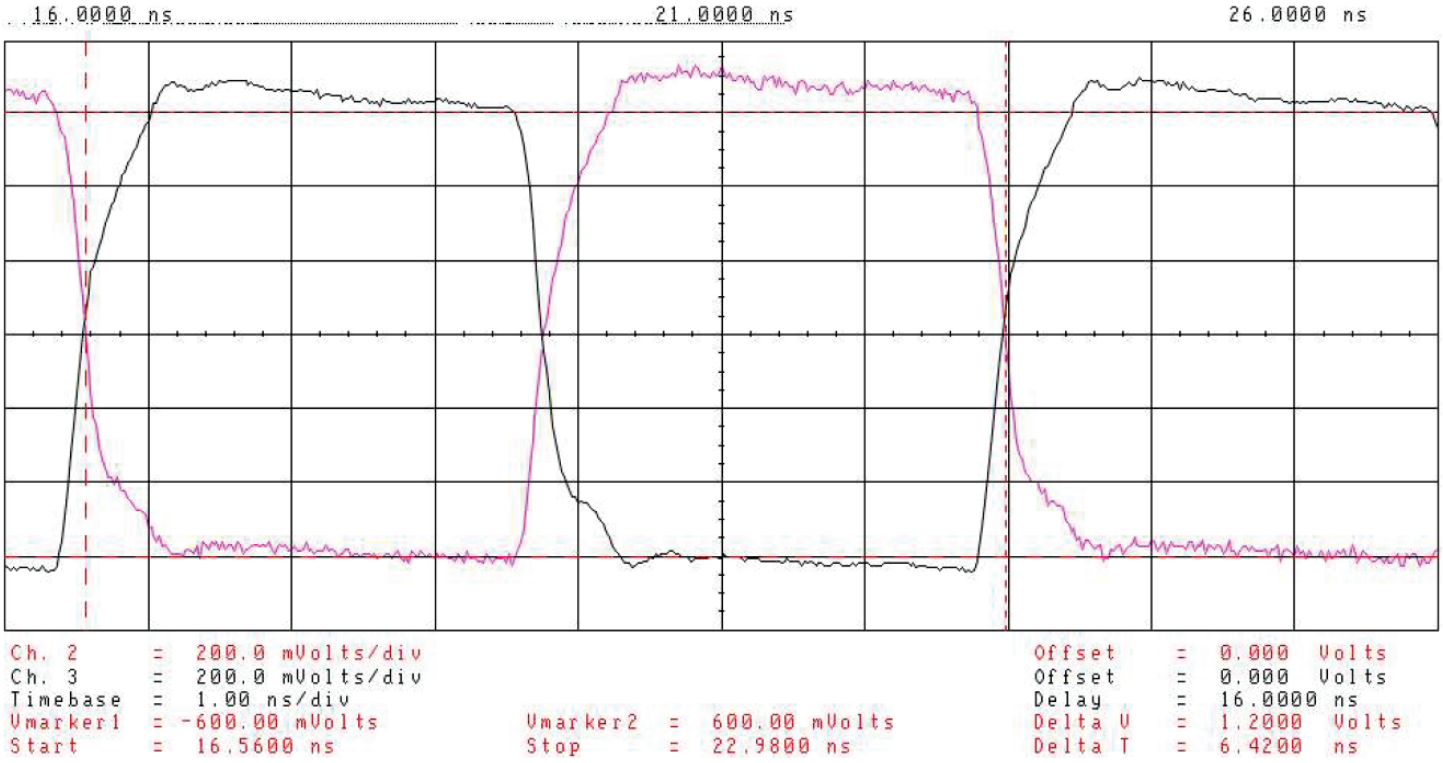


Figure 9 156MHz Output Waveforms - 150Ω DC Load

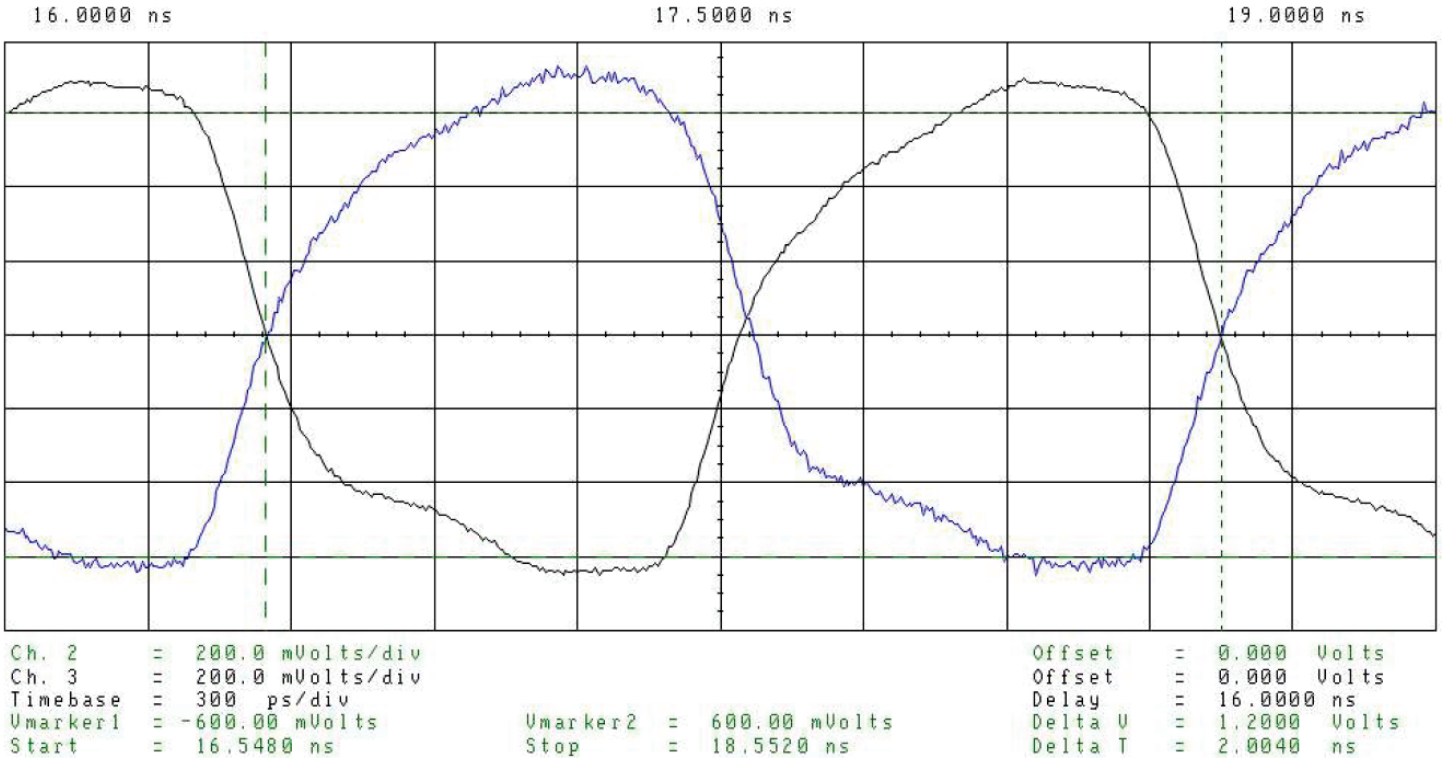


Figure 10 500 MHZ Output Waveforms - 150Ω DC Load

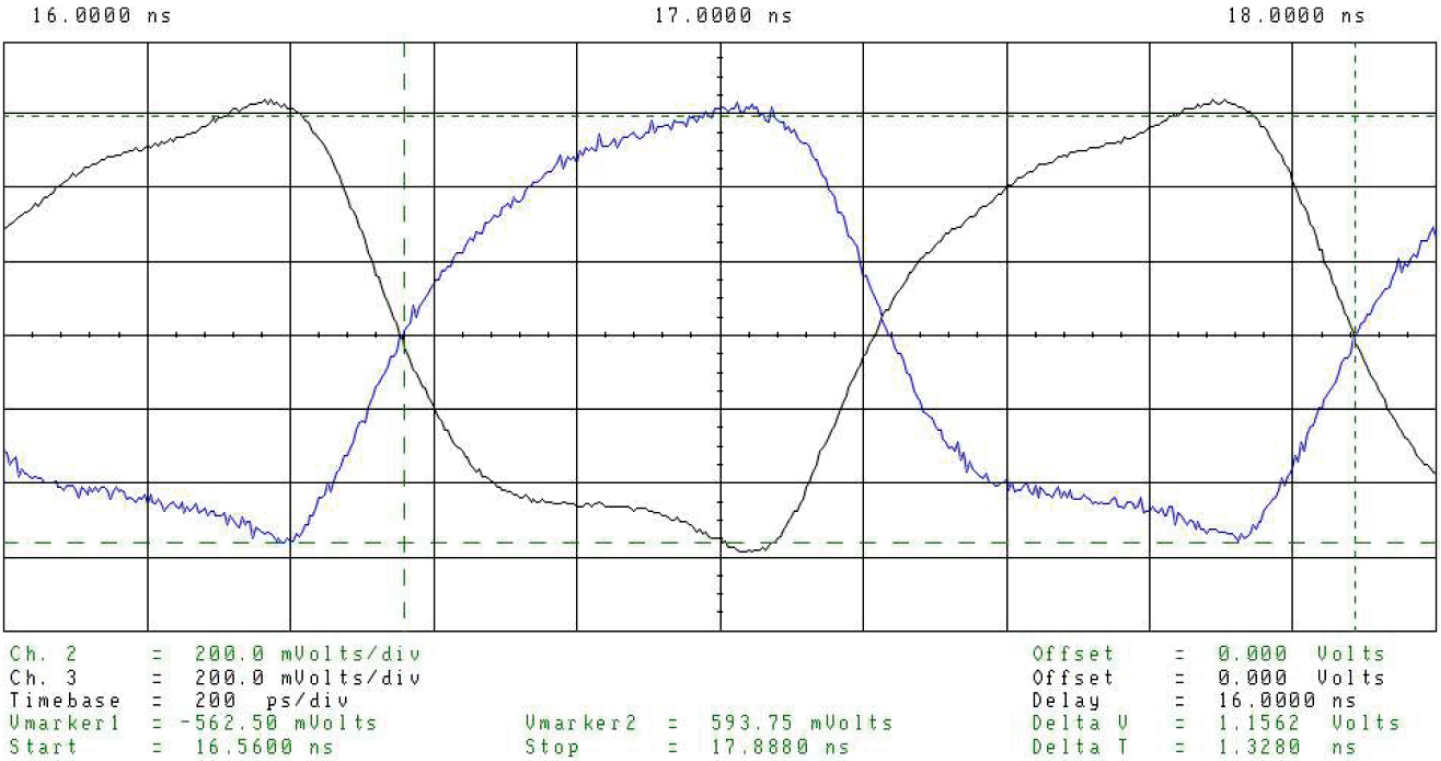


Figure 11 750MHz Output Waveforms - 150Ω DC Load

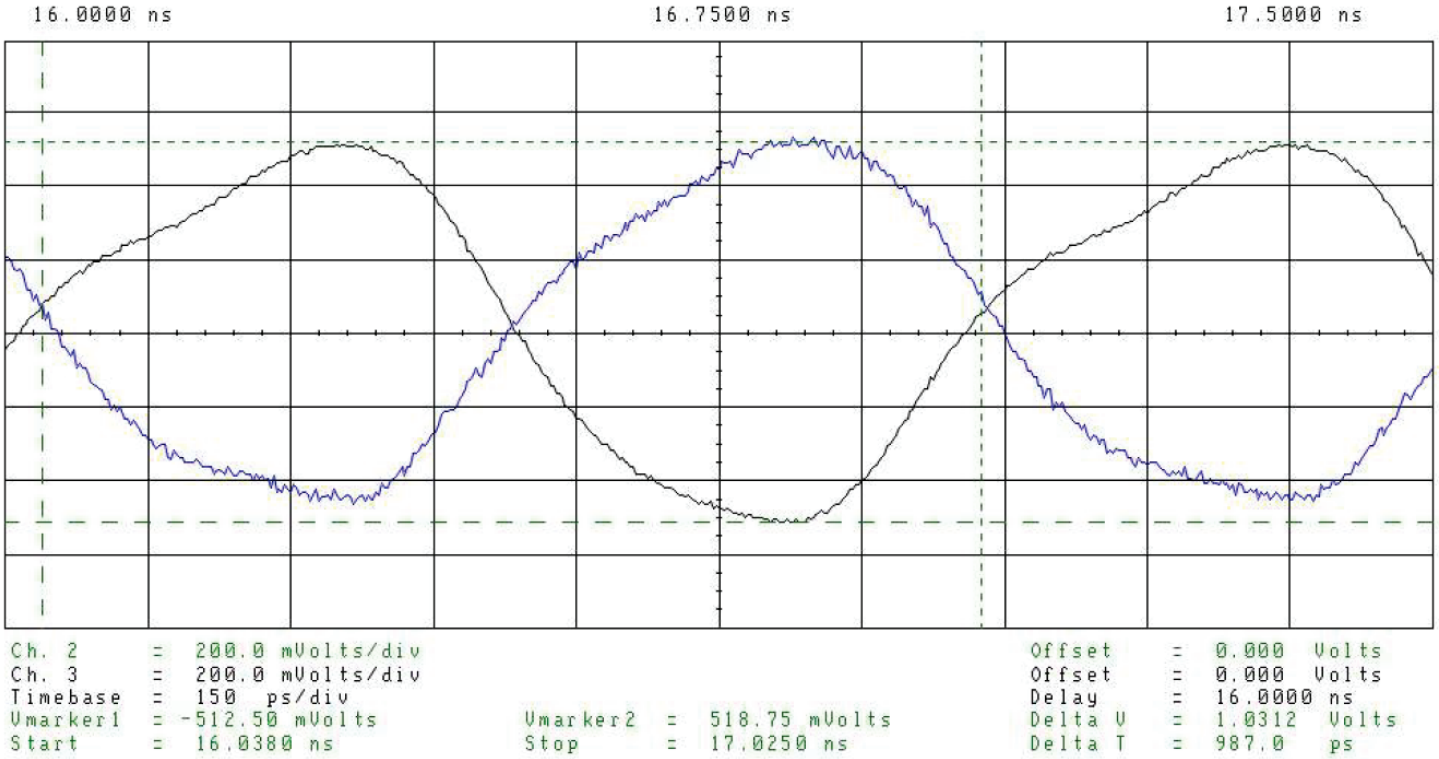


Figure 12 1GHz Output Waveforms - 150Ω DC Load

APPLICATION NOTES

Input Terminations

Sine Wave Input Termination

Figure 13 illustrates the circuit configuration for applying a single-ended sinewave signal to the input of the CF112P. A 50Ω resistor is necessary to match the AC line impedance while the resistor network on the CF112P side of the coupling capacitor is used to set a VDD/2 midpoint DC bias for optimal switching.

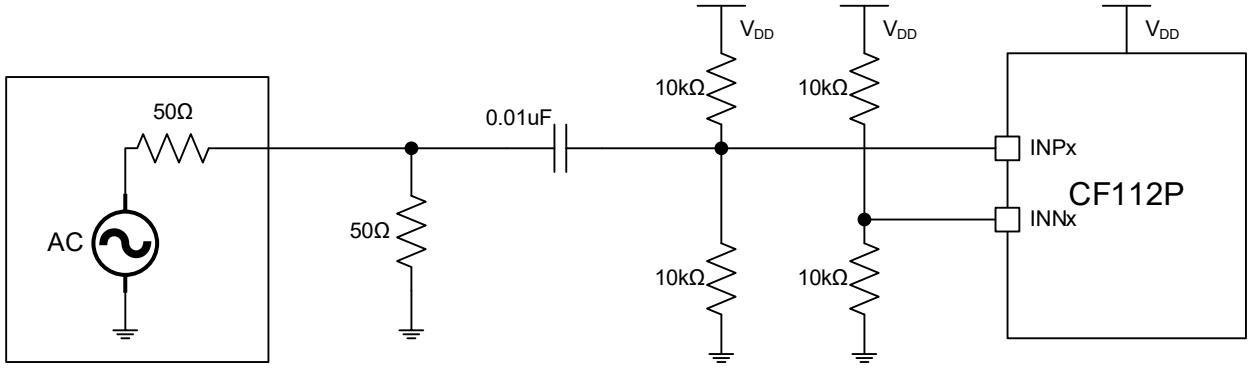


Figure 13 AC Coupled Sine Wave Termination

CMOS Input Termination

Figure 14 illustrates the circuit configuration for applying a single-ended CMOS signal to the input of the CF112P. With a full amplitude CMOS signal connected directly into the input receiver, only the input complement needs to be considered. The resistor network is used to set a VDD/2 midpoint DC bias for optimal switching while the capacitor filters out high frequency supply noise.

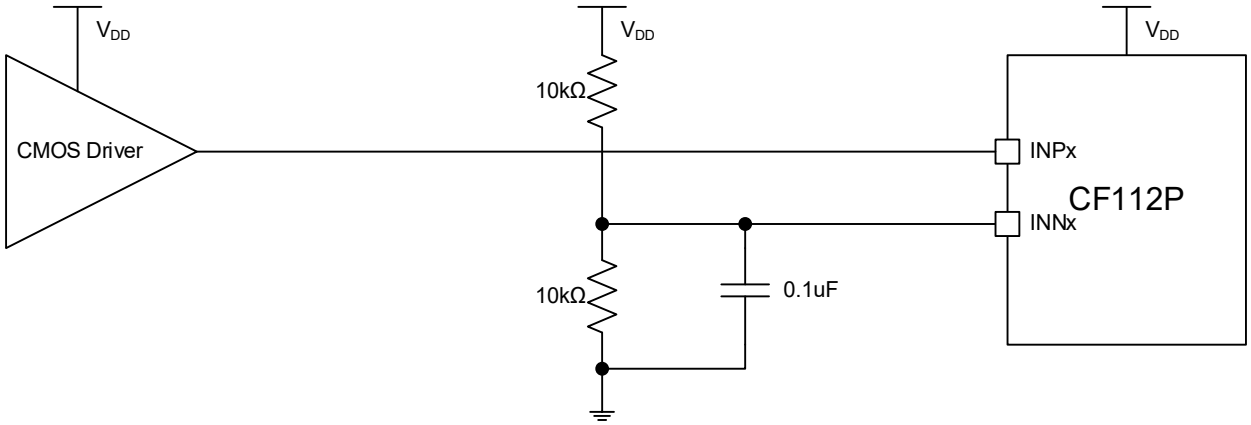


Figure 14 DC Coupled CMOS Termination

LVPECL Input Termination

Figure 15 illustrates the Thevenin equivalent circuit configuration for terminating a LVPECL driver and DC coupling the signal to the input of the CF112P. Each resistor network value is equal to the transmission line's characteristic impedance (50Ω).

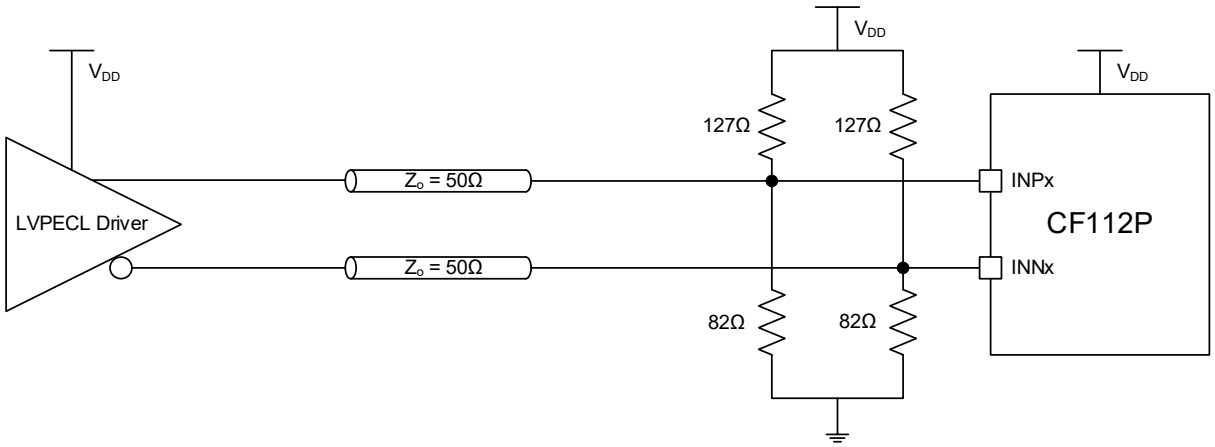


Figure 15 DC Coupled LVPECL Termination

Figure 16 illustrates AC coupling a differential LVPECL signal to the input of the CF112P. Each resistor network value is equal to the transmission line's characteristic impedance (50Ω). R1 sets the DC load of the LVPECL driver.

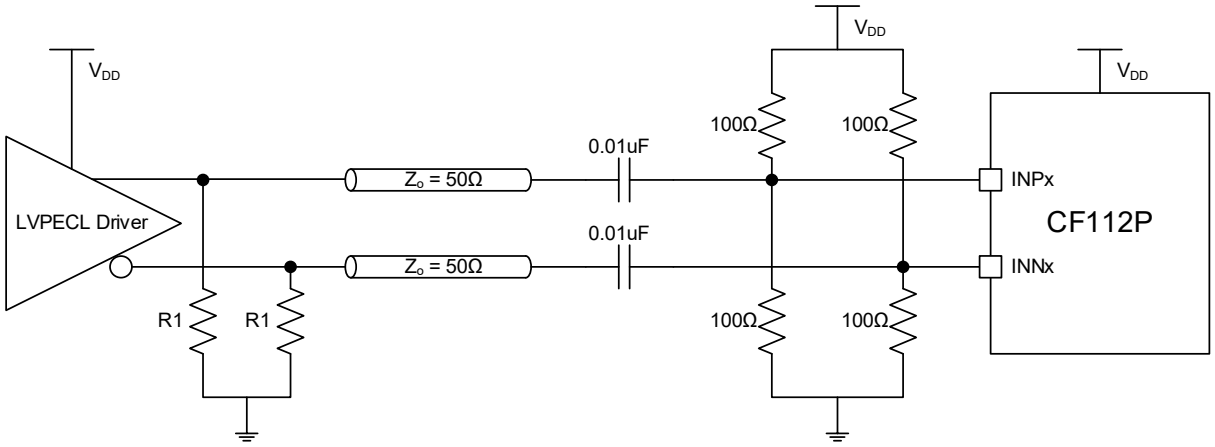


Figure 16 AC Coupled LVPECL Termination

LVDS Input Termination

Figure 17 shows an LVDS termination for DC coupling the differential LVDS signal to the input of the CF112P.

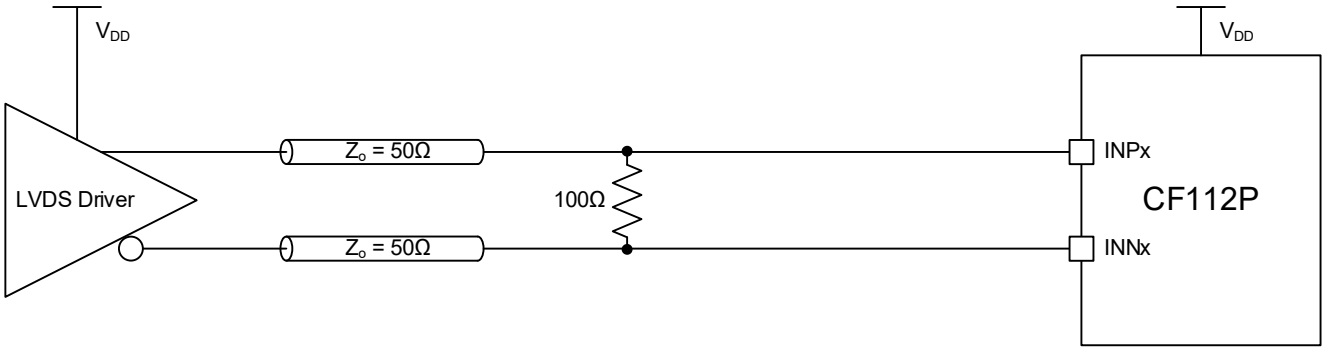


Figure 17 DC Coupled LVDS Termination

Figure 18 shows an LVDS termination for AC coupling the differential LVDS signal to the input of the CF112P.

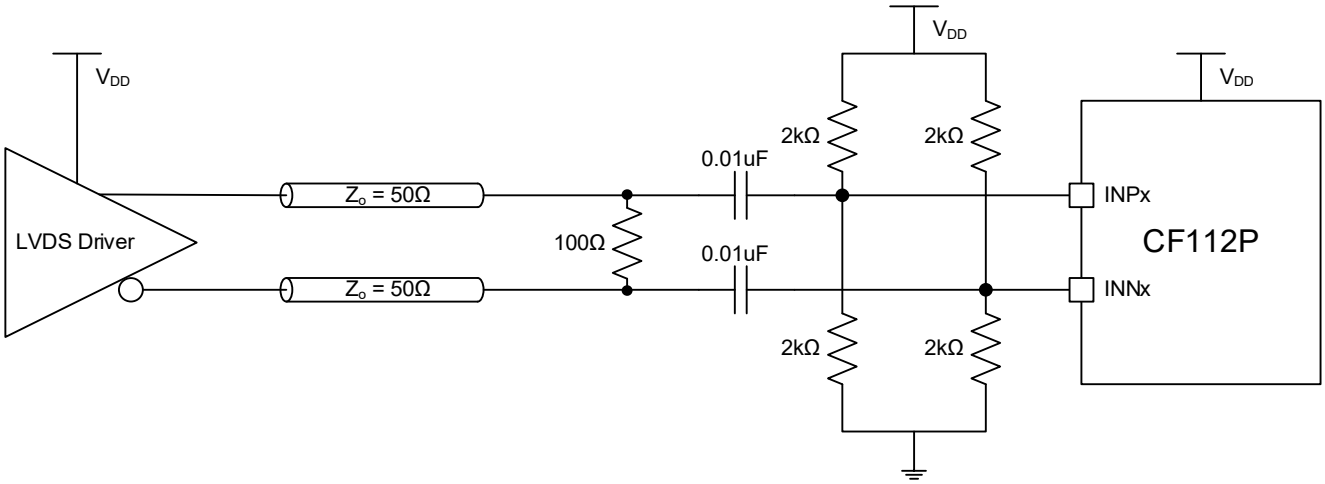


Figure 18 AC Coupled LVDS Termination

Output Terminations

AC Output Termination

Clock applications or phase noise/frequency domain testing scenarios typically require AC coupling. Figure 19 below shows the AC coupling technique. The R1 resistors form the required DC loads, and the 50Ω resistors provide the AC termination. The parallel combination results in the net AC load termination. In many cases, R1 values between 100Ω-200Ω work well. Alternately, bias tees combined with current setting resistors will eliminate the lowered AC load impedance. The 50Ω resistors are typically connected to ground but can be connected to the bias level needed by the succeeding stage.

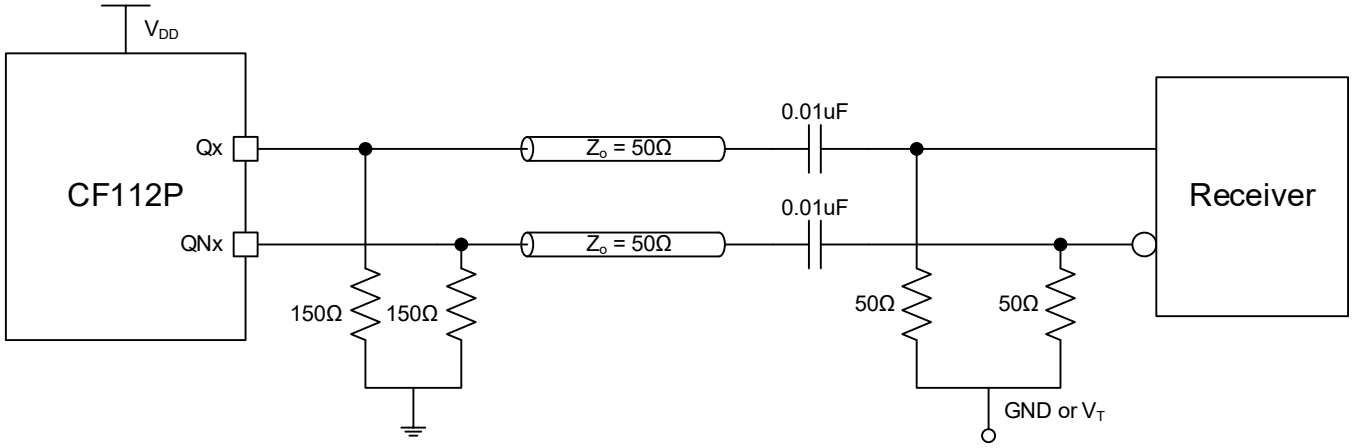


Figure 19 AC Coupled LVPECL Output Termination (Recommended)

DC Output Termination

The CF112P uses a current drive topology to maximize switching speed as illustrated below in Figure 2. Figure 20 illustrates the often-preferred Thevenin equivalent circuit configuration for terminating the CF112P LVPECL driver. The associated output voltage swings match LVPECL levels when external 50Ω resistors terminate the outputs. Both Q and QN should always be terminated identically to avoid waveform distortion and circulating current caused by unsymmetrical loads. This rule should be followed even if only one output is in use.

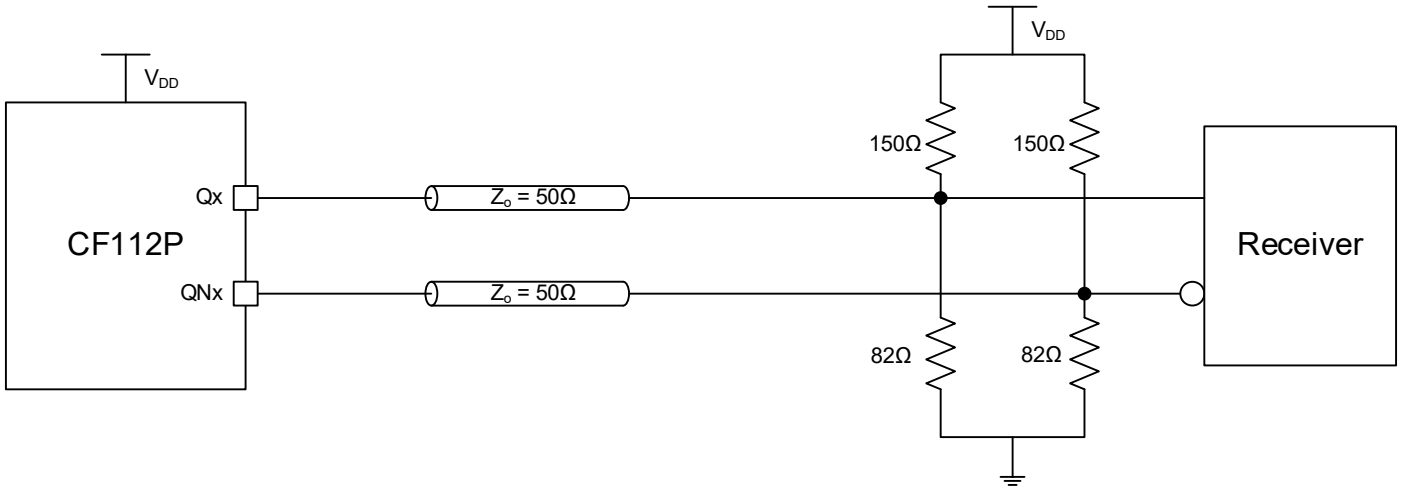


Figure 20 DC Coupled LVPECL Output Termination

Single Edge Clock Applications

Some applications of the CF112P drive single clock edge sensitive devices such as some analog-to-digital converters. Each edge of the output waveform must be stable without additional added jitter for excellent performance in those applications.

The plot shows the phase noise performance of the CF112P fed from a 125 MHz low noise oscillator, in a divide by one circuit and an edge sensitive divide by 2 circuit. Edge dependent jitter would show a “hump” in the phase noise curve at 62.5MHz. The phase noise floor is set by the 125 MHz oscillator, and the 1/f noise at 62.5 MHz decreases by 6 dB as expected.

The overlapping phase noise curves show that the CF112P does not exhibit edge dependent jitter and will provide excellent performance when driving a single edge sensitive device.

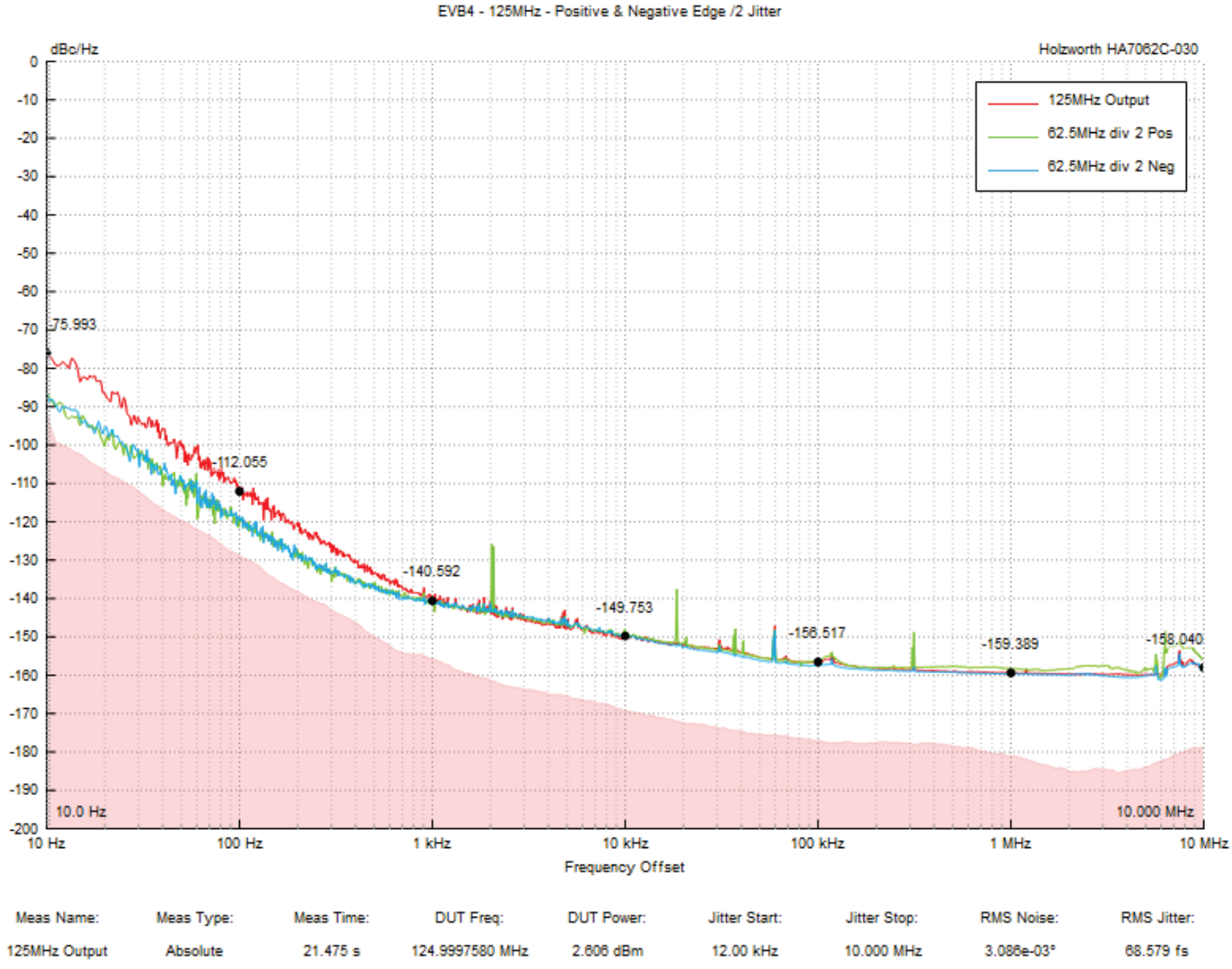


Figure 21 Edge Dependent Phase Noise

PCB CONSIDERATIONS

Power Supply Filtering

On-chip regulation, power supply filtering and good PCB layout all contribute to minimizing the additive jitter from the power supply noise. For optimal performance the CF112P should be isolated from the power supply noise with the following guidelines:

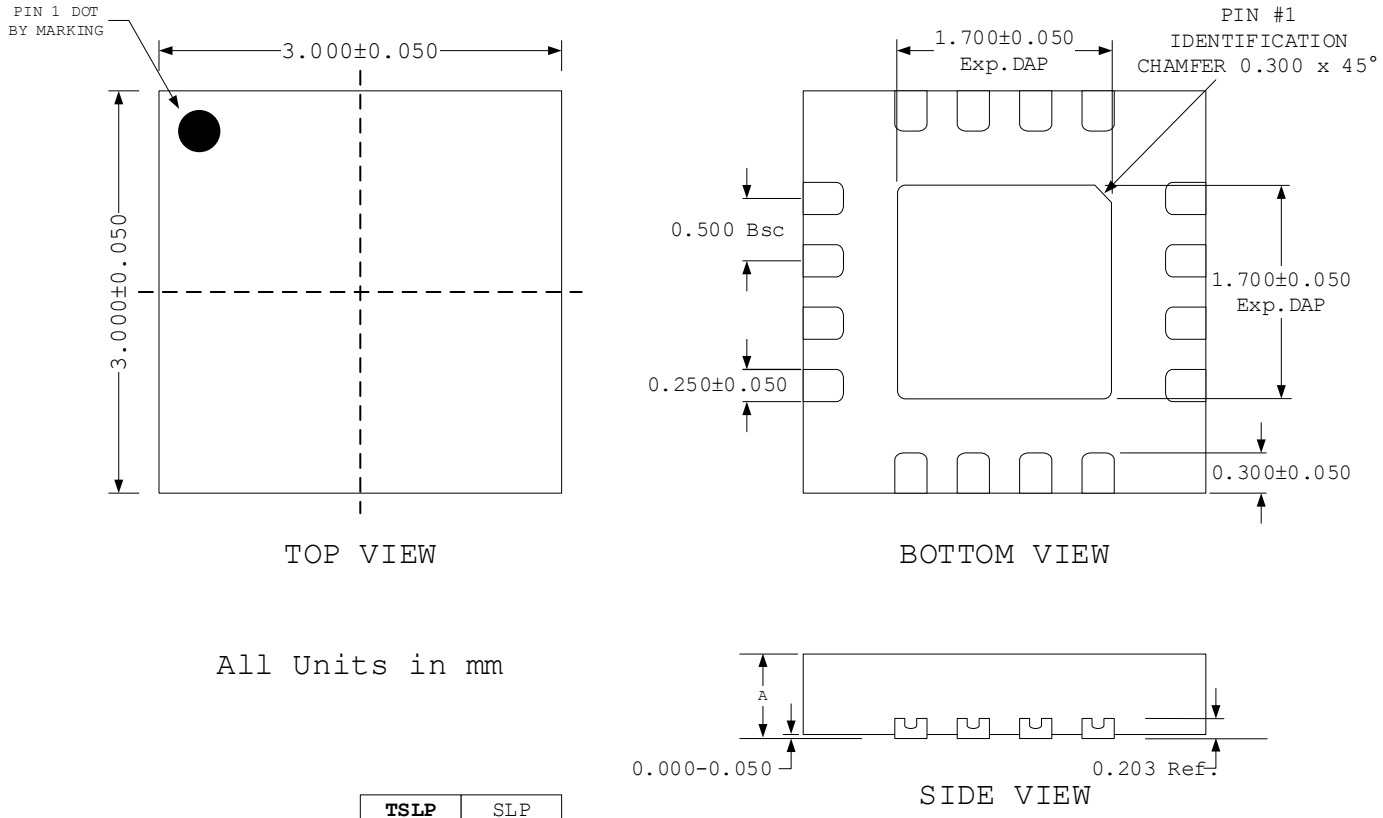
1. Power supply traces need to be appropriately sized for the high current demands. Consider parallel power supply routes (star routing) to each of the output supply pins (VDDOx) which can pull up to 60mA each.
2. Place a 22uF bypass capacitor from the power supply to the device's supply pins. A 1206 or larger X7R ceramic or tantalum capacitor is recommended.
3. Place a 0.01uF bypass capacitor from the power supply to the device's supply pins. A 0402 or 0603 X7R ceramic capacitor is recommended.
4. One set of bypass capacitors (22uF & 0.01uF) is sufficient if placed before the main power supply trace splits to the VDDOx pins. Bypass capacitors, however, should be placed as close as possible to the device.
5. Consider also placing a ferrite bead in series with the power supply to the device's supply pin.

Signal Traces

Improper routing of the signals of the CF112P can have adverse effects on the additive jitter performance and therefore must be treated with care. Signals should not be treated as digital signals but rather high-performance analog signals otherwise system performance may be degraded. Signal routing guidelines include:

1. Physically locate the signal source as close to the load as possible
2. Limit the length of clock traces
3. Do not run signals through or near large FPGAs (or similar) with lots of switching activity and various frequencies
4. Do not run signals adjacent to digital data lines
5. Avoid routing signals near or alongside digital lines
6. Avoid crossing digital traces on an adjacent PCB planes
7. Shield signals with ground planes, adjacent traces, or both
8. Try to keep clock trace routes straight; if turns are necessary, make them with round bends

PACKAGE OUTLINE



		TSLP	SLP
A	MAX	**0.800**	0.900
	NOM	**0.750**	0.850
	MIN	**0.700**	0.800

Figure 22 Packing Outline

DEVICE MARKING

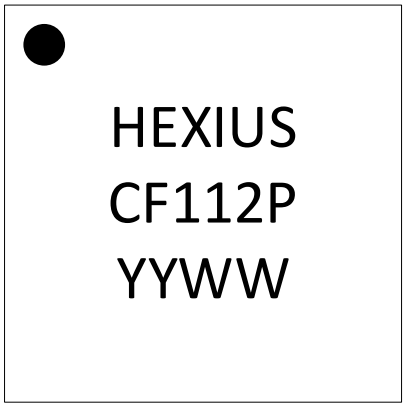


Figure 23 Device Marking

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